

## Molded, 50 mil Pitch, Dual-In-Line Thin Film Resistor, Surface Mount Network



ORN series resistor networks feature four isolated resistors with standard 50 mil pitch lead spacing. The networks feature close TCR tracking and tight ratio tolerance and are ideally suited for unity gain operational amplifier circuitry. The standard resistance offering listed are available for immediate delivery.

### SCHEMATIC



### FEATURES

- 0.068" (1.73 mm) maximum seated height
- Rugged molded case construction with no internal solder
- Low temperature coefficient ( $\pm 25$  ppm/ $^{\circ}$ C)
- JEDEC MS-012 STD variation AA package
- Compliant to RoHS Directive 2002/95/EC
- Halogen-free according to IEC 61249-2-21 definition



**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**

### Note

- \* Pb containing terminations are not RoHS compliant, exemptions may apply

### TYPICAL PERFORMANCE

	ABSOLUTE	TRACKING
TCR	25	5
	ABSOLUTE	RATIO
TOL.	0.1	0.05

### STANDARD RESISTANCE OFFERING ( $R_1 =$ )

49.9 $\Omega$	10 k $\Omega$
100 $\Omega$	20 k $\Omega$
500 $\Omega$	50 k $\Omega$
1 k $\Omega$	100 k $\Omega$
2 k $\Omega$	200 k $\Omega$
4.99 k $\Omega$	500 k $\Omega$
5 k $\Omega$	

### Note

- Consult factory for additional values and schematics

STANDARD ELECTRICAL SPECIFICATIONS		
TEST	SPECIFICATIONS	CONDITIONS
Material	Passivated nichrome	-
Pin/Lead Number	8	-
Resistance Range	33 $\Omega$ to 500 k $\Omega$ per resistor	-
TCR: Absolute	$\pm 25$ ppm/ $^{\circ}$ C	- 55 $^{\circ}$ C to + 125 $^{\circ}$ C
TCR: Tracking	$\pm 5$ ppm/ $^{\circ}$ C	- 55 $^{\circ}$ C to + 125 $^{\circ}$ C
Tolerance: Absolute	$\pm 0.05$ % to $\pm 1.0$ %	+ 25 $^{\circ}$ C
Tolerance: Ratio	$\pm 0.01$ % to $\pm 0.5$ %	+ 25 $^{\circ}$ C
Power Rating: Resistor	100 mW	Maximum at + 70 $^{\circ}$ C
Power Rating: Package	400 mW	Maximum at + 70 $^{\circ}$ C
Stability: Absolute	$\Delta R \pm 0.05$ %	2000 h at + 70 $^{\circ}$ C
Stability: Ratio	$\Delta R \pm 0.015$ %	2000 h at + 70 $^{\circ}$ C
Voltage Coefficient	0.1 ppm/V (typical)	-
Working Voltage	100 V max. not to exceed $\sqrt{P \times R}$	-
Operating Temperature Range	- 55 $^{\circ}$ C to + 125 $^{\circ}$ C	-
Storage Temperature Range	- 55 $^{\circ}$ C to + 150 $^{\circ}$ C	-
Noise	< - 30 dB	-
Thermal EMF	0.08 $\mu$ V/ $^{\circ}$ C	-
Shelf Life Stability: Absolute	$\Delta R \pm 0.01$ %	1 year at + 25 $^{\circ}$ C
Shelf Life Stability: Ratio	$\Delta R \pm 0.002$ %	1 year at + 25 $^{\circ}$ C

**DIMENSIONS AND IMPRINTING** in inches and millimeters

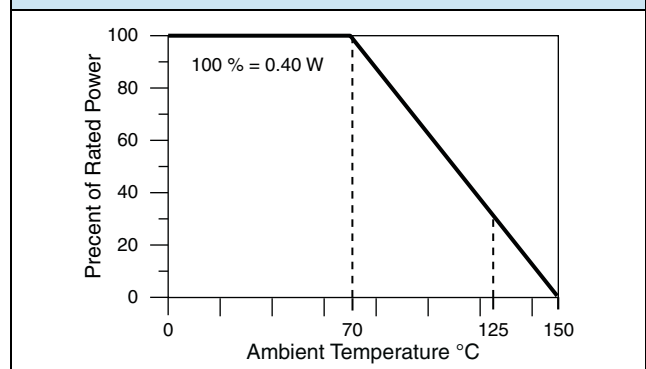

DIMENSION	INCHES	MILLIMETERS
A	0.157	3.99
B	0.0165 ± 0.0025	0.4 ± 0.06
C	0.050	1.27
D	0.195 max.	4.93
E	0.008 ± 0.001	0.20 ± 0.03
F	0.028 ± 0.001	0.71 ± 0.02
G	0.239 ± 0.005	6.07 ± 0.13
H	0.068 max.	1.73
I	0.008 ± 0.002	0.22 ± 0.06
Ø	2° to 6°	2° to 6°

**Note**

- Marking - Vishay symbol, part number from ordering information

**MECHANICAL SPECIFICATIONS**

Resistive Element	Passivated nichrome
Substrate Material	Silicon
Body	Molded epoxy
Terminals	Copper alloy
Lead (Pb)-free Option	100 % matte tin
Tin Lead Option	Sn90
Tin Lead and Lead (Pb)-free Finish	Plated

**DERATING CURVE**

**GLOBAL PART NUMBER INFORMATION**

New Global Part Numbering: ORNA1002AUF



GLOBAL MODEL (3 or 4 digits)	SCHEMATIC	RESISTANCE	TOLERANCE AND RATIO TOLERANCE	PACKAGING																
<b>ORN</b> (Tin lead)  <b>ORNT</b> (Lead (Pb)-free) (e3)	<b>A</b> = 4 isolated equal resistors	The first 3 digits are significant figures and the last digit specifies the number of zeros to follow. R designates the decimal point.  Example: 1002 = 10 kΩ 1003 = 100 kΩ 4991 = 4.99 kΩ 50R0 = 50 Ω	<table border="1"> <thead> <tr> <th>Abs. Tol.</th> <th>Ratio</th> </tr> </thead> <tbody> <tr> <td><b>A</b> = ± 0.1 % <sup>(3)</sup></td> <td>± 0.05 %</td> </tr> <tr> <td><b>B</b> = ± 0.1 %</td> <td>± 0.1 %</td> </tr> <tr> <td><b>C</b> = ± 0.25 %</td> <td>± 0.1 %</td> </tr> <tr> <td><b>D</b> = ± 0.5 %</td> <td>± 0.1 %</td> </tr> <tr> <td><b>F</b> = ± 1 %</td> <td>± 0.5 %</td> </tr> <tr> <td><b>Q</b> = ± 0.05 % <sup>(1)</sup></td> <td>± 0.01 %</td> </tr> <tr> <td><b>Z</b> = ± 0.1 % <sup>(1)</sup></td> <td>± 0.025 %</td> </tr> </tbody> </table>	Abs. Tol.	Ratio	<b>A</b> = ± 0.1 % <sup>(3)</sup>	± 0.05 %	<b>B</b> = ± 0.1 %	± 0.1 %	<b>C</b> = ± 0.25 %	± 0.1 %	<b>D</b> = ± 0.5 %	± 0.1 %	<b>F</b> = ± 1 %	± 0.5 %	<b>Q</b> = ± 0.05 % <sup>(1)</sup>	± 0.01 %	<b>Z</b> = ± 0.1 % <sup>(1)</sup>	± 0.025 %	TAPE AND REEL <b>T0</b> = 100 min., 100 mult <b>T1</b> = 1000 min., 1000 mult <sup>(2)</sup> <b>T3</b> = 300 min., 300 mult <b>T5</b> = 500 min., 500 mult <b>TF</b> = Full reel 3000 <b>TS</b> = 100 min., 1 mult  <b>UF</b> = TUBED
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Historical Part Number example: ORNA1001F (for reference purposes only)																				
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**Notes**

- Tol. available 1K and up
- Preferred packaging code
- Ratio tolerance available 250 Ω and up



### Vishay Dale Thin Film Land Patterns

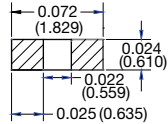
#### 1. Scope

This technical note provides sample land patterns for Vishay Dale Thin Film SMT resistive products. The following drawings are based on IPC-SM-782 Surface Mount Design and Land Pattern Standard. These drawings are for reference only Vishay Thin Film recommends that the user contacts their PC board supplier for actual land patterns required. The pads are intended for lead (Pb)-free and tin / lead solder types.

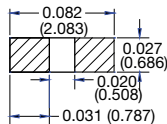
#### 2. Product Series

Thin Film Surface Mount Chip Resistors (FC, L, P, PTN, PLT, PLTT, PLTU, PAT, PATT, PNM, M/D55342 QPL Series)

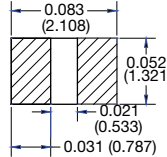
**0402 Land Pattern**



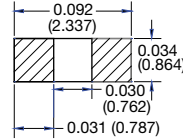
**0502 Land Pattern**



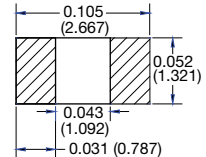
**0505 Land Pattern**



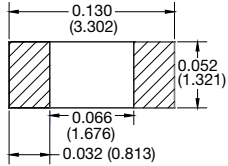
**0603 Land Pattern**



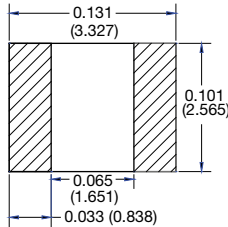
**0705 Land Pattern**



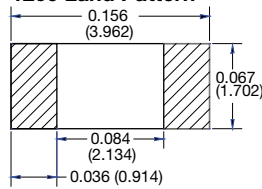
**1005 Land Pattern**



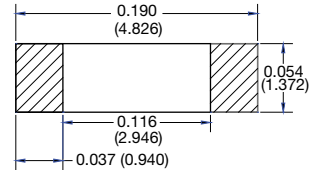
**1010 Land Pattern**



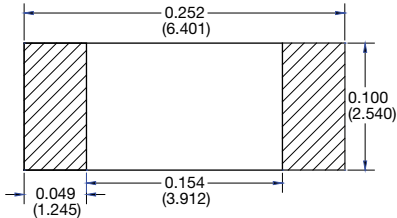
**1206 Land Pattern**



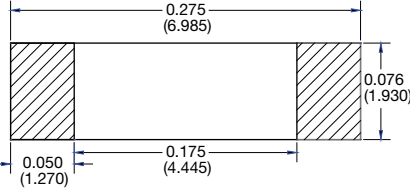
**1505 Land Pattern**



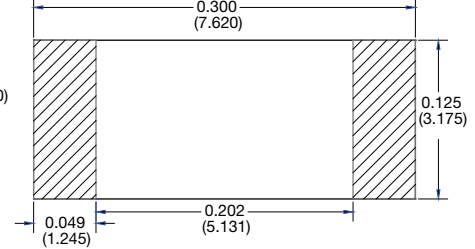
**2010 Land Pattern**



**2208 Land Pattern**

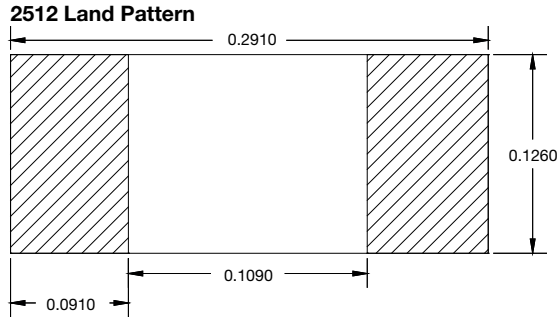
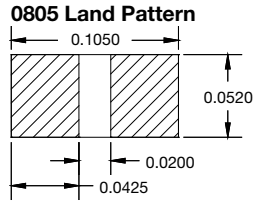
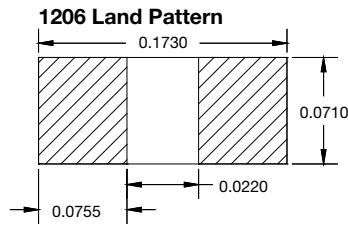
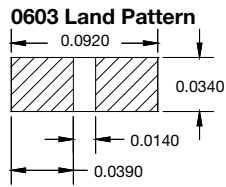


**2512 Land Pattern**

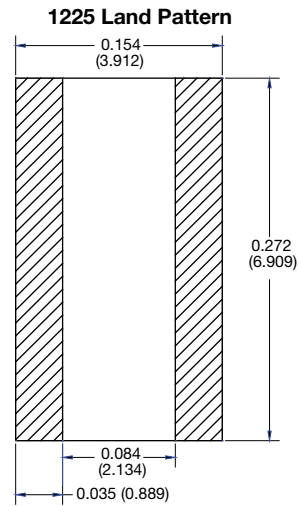
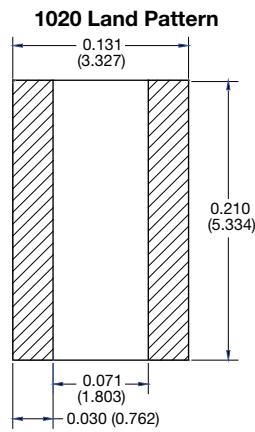
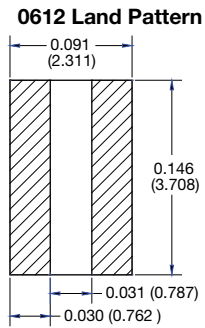
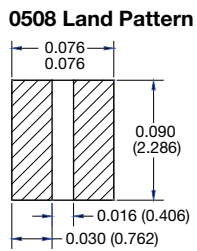




## Thin Film Surface Mount Chip Resistors (PHP, PCAN Series)

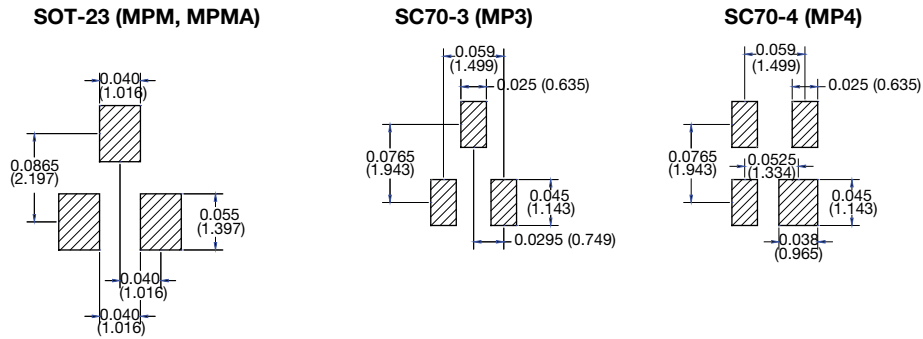


## Thin Film Surface Mount Chip Resistors Long Axis Termination (L Series)

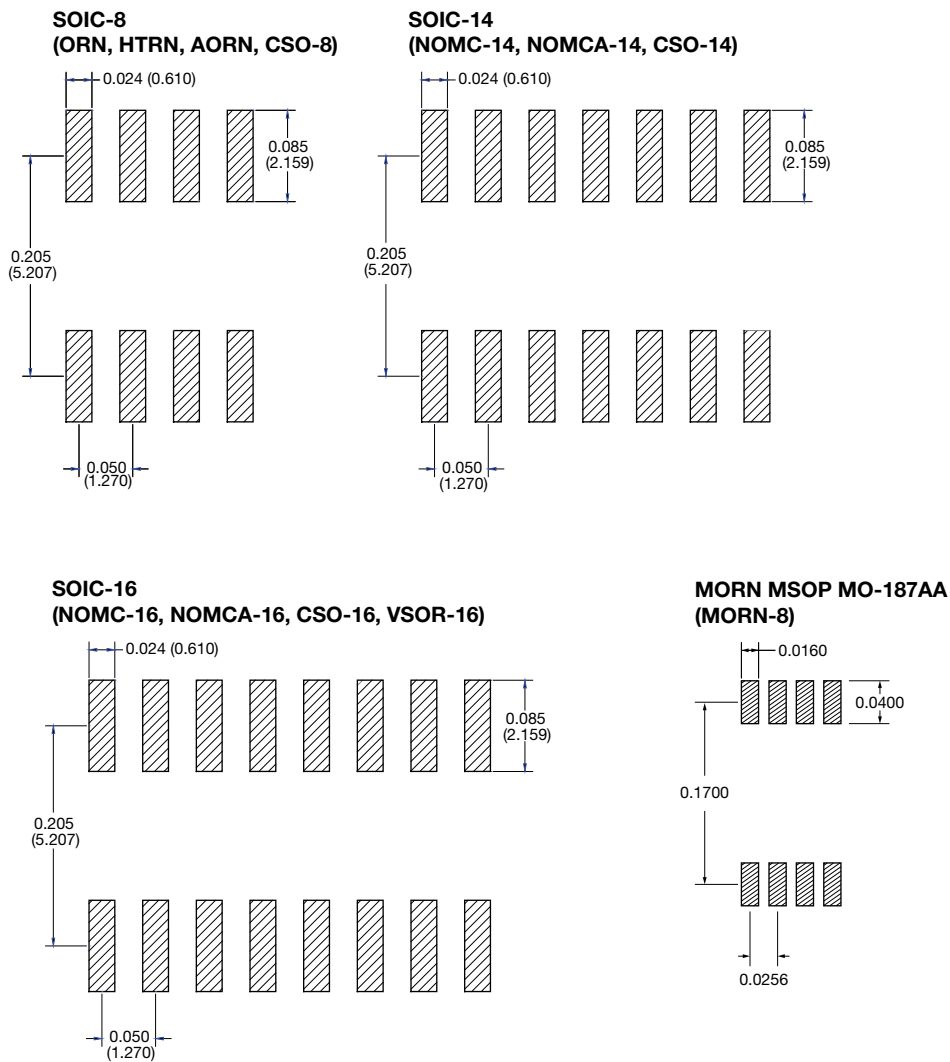




### Surface Mount Networks (MPM, MP3, MP4 Series)

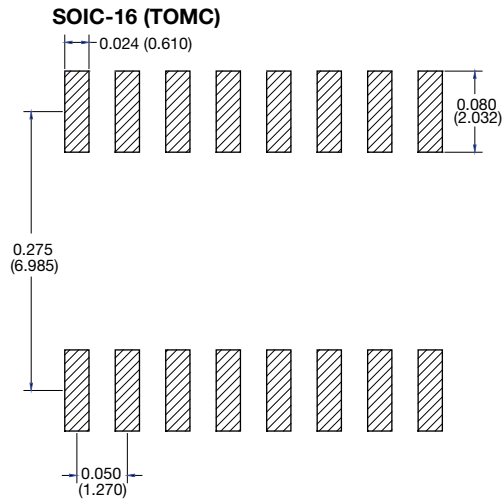


### Surface Mount Networks SOIC Narrow Body 150 mils (ORN, CSO, MOMC, HTRN, AORN, MORN Series)

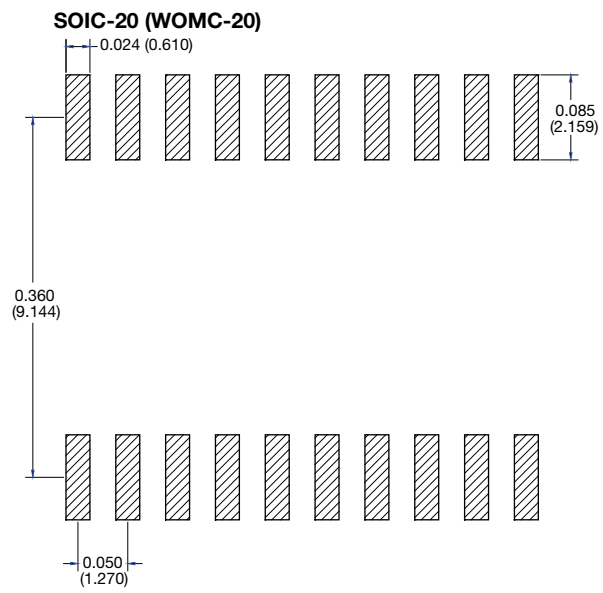
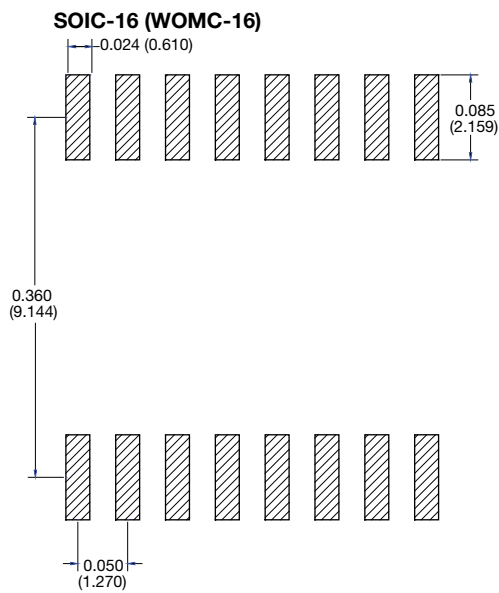




### Surface Mount Networks SOIC Medium Body 220 mils (TOMC Series)



### Surface Mount Networks SOIC Wide Body 300 mils (WOMC Series)

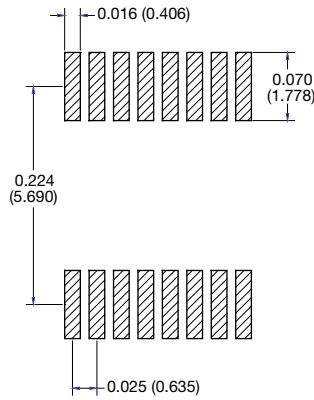




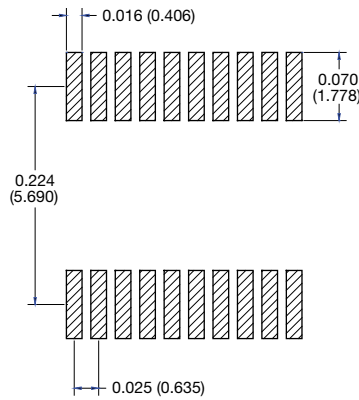
### Surface Mount Networks High Density SSOP, TSOP (VSSR, VTSR Series)

#### SSOP MO-137

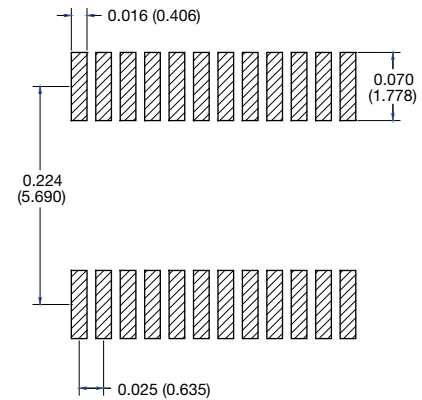
##### OSOP-16, VSSR-16



##### OSOP-20, VSSR-20

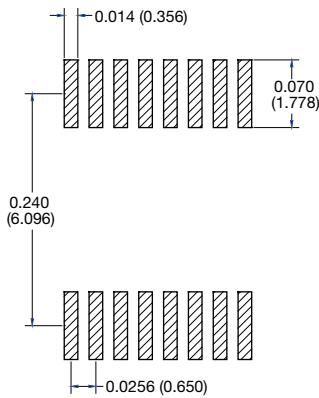


##### OSOP-24, VSSR-24, HD-CSO-24

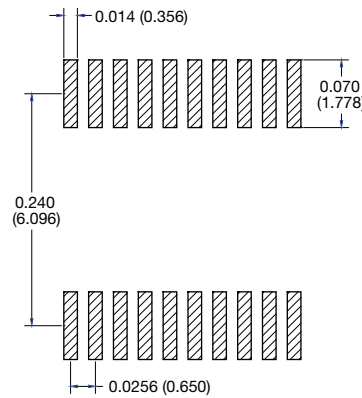


#### TSSOP MO-153

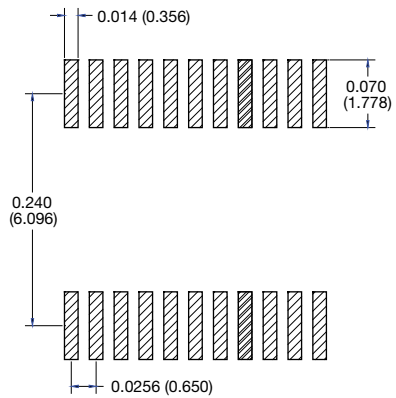
##### VTSR-16



##### VTSR-20

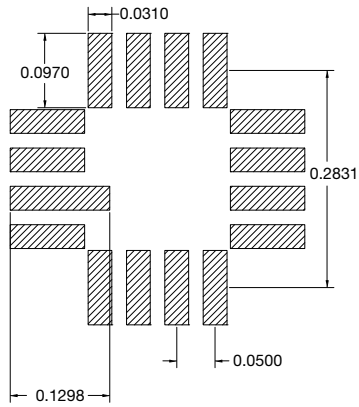


##### VTSR-24

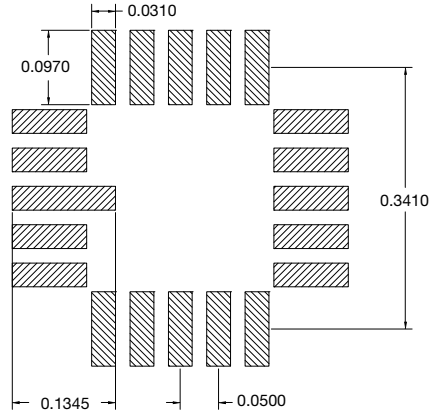


Surface Mount Leadless Networks (LCC Series)

**16 Pin LCC**

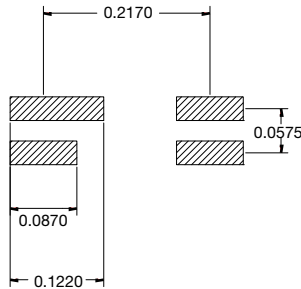


**20 Pin LCC**



Surface Mount Leadless Networks (MPH Series)

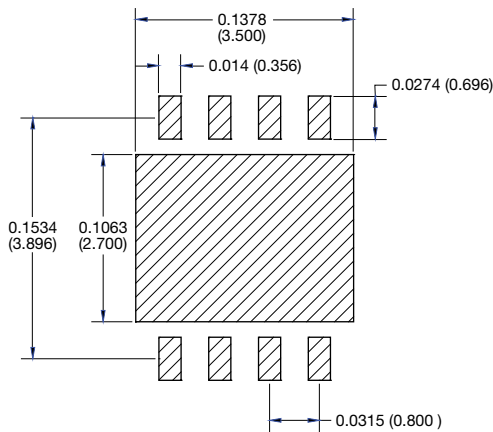
**4 Pin LCC**



Surface Mount Leadless Packages DUAL/ QUAD Flat No Lead (DFN, QFN Series)

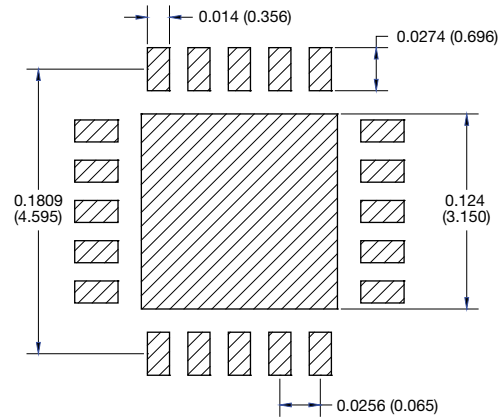
**DFN MLP**

**DFN-8 4 x 5 mm Sq**



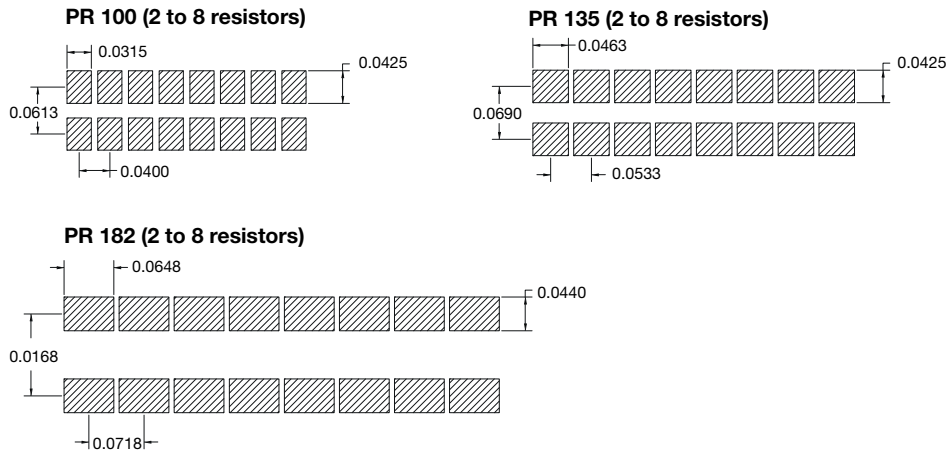
**QFN MLP**

**QFN-20 5 x 5 mm Sq**





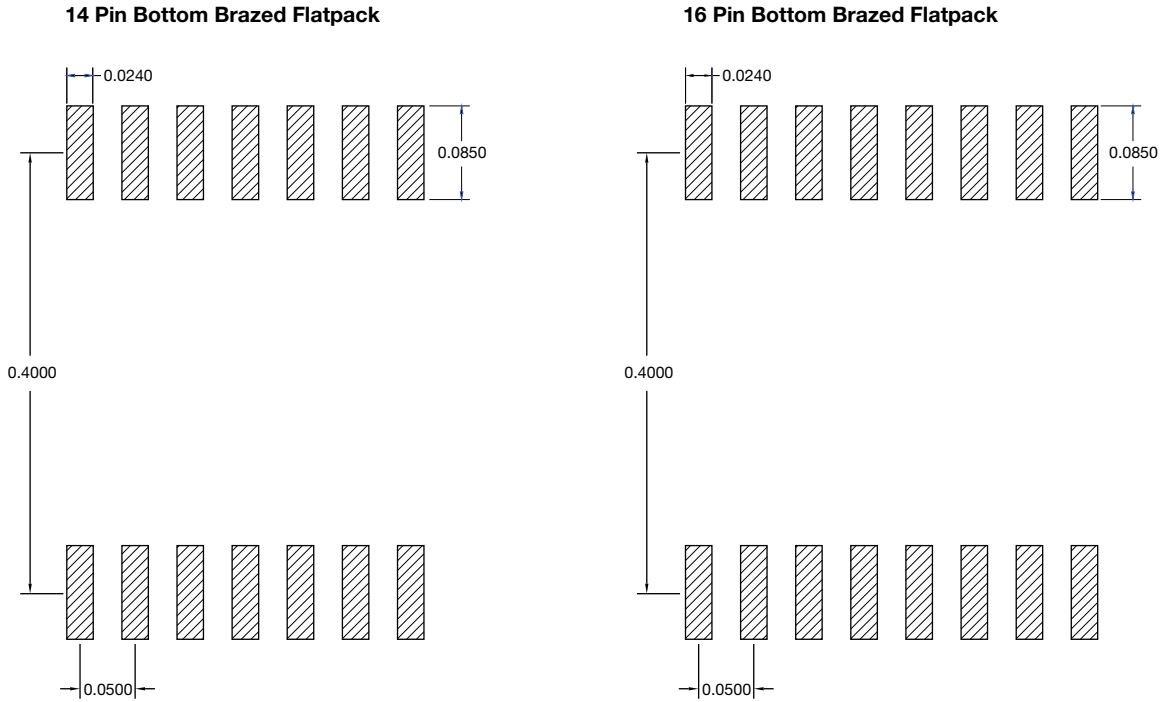
### Surface Mount Leadless Resistor Arrays (PR Series)



**Note**

- All dimensions in inches (mm)

### Flatpack





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