



Vishay Thin Film Engineering Test Report

PLT CHIP RESISTOR - SURGE IMMUNITY TESTING

1. Background

Surge immunity or electromagnetic compatibility can be defined as a system or device's ability to withstand continuous or pulsed/transient energy from external sources without having adverse affect on its' performance. In this testing we conducted pulse or transient surge immunity testing in order to understand how Vishay Thin Film's PLT product line would perform over a range of transient voltage levels.

2. Experimental Methods

Surge immunity testing, for this study, was conducted according to IEC standard 60115-1, paragraph 4.27 using the 1.2/50 μ s waveform. Samples for the testing were selected from 3 different case sizes and multiple values as detailed in table 1 below.

TABLE 1 - SAMPLE DETAILS				
CASE SIZE	RESISTANCE VALUE			
0603	301 Ω	1 k Ω	10 k Ω	25 k Ω
1206	250 Ω			50 k Ω
2512	100 Ω	12.3 k Ω	50 k Ω	100 k Ω

To facilitate the application of voltage pulses to the device under test (DUT), samples were mounted to FR-4 test cards and inserted into a testing fixture as shown in figure 1 below.

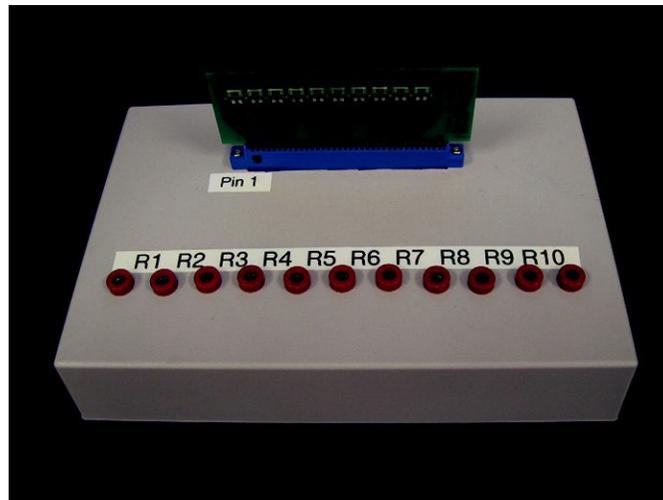


Fig. 1 - Test Fixture

Voltage pulses, following the 1.2/50 μ s, waveform were generated using a Schaffner NSG650 High Energy Pulse Generator. Prior to conducting the testing, the voltage waveform was verified using a Tektronix TDS3034B oscilloscope. This measured waveform is shown in figure 2. Based on scaling, each 200 mV division shown below is equivalent to 200 V.

Vishay Thin Film Engineering Test Report

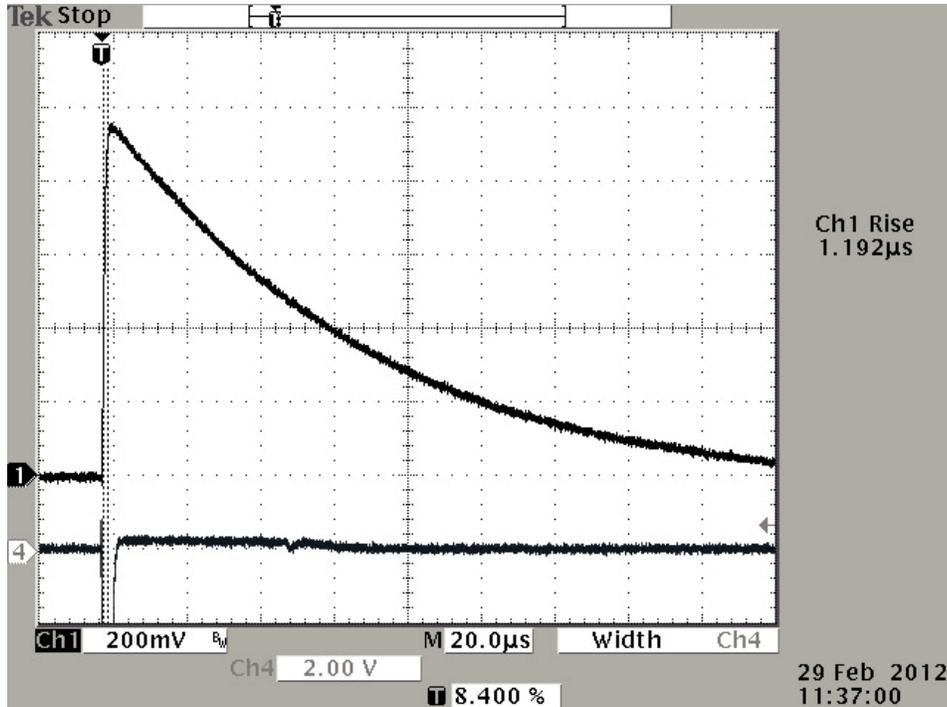


Fig. 2 - 1.2/50 µs Waveform Verification

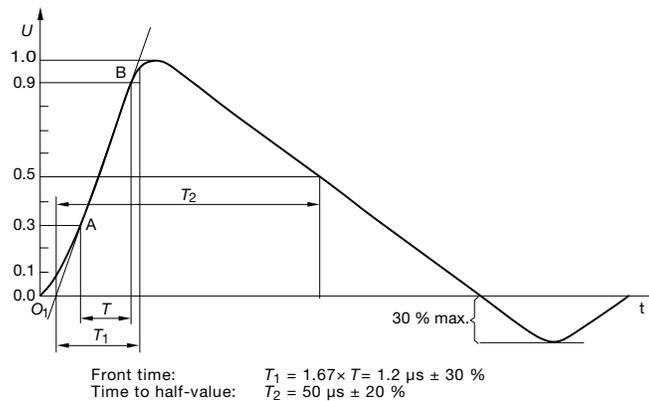


Fig. 3 - Waveform of Open-circuit Voltage (1.2/50 µs) at the Output of the Generator with no CDN connected (waveform definition according to IEC 60060-1)

TECHNICAL NOTE

Testing was conducted by subjecting sample groups of 10 resistors, individually, to incrementally higher voltage pulses, starting with 200 V, until a resistance delta greater than 0.5 % was observed. New samples were used for each voltage pulse level.

Due to the pulse generator lower voltage limit of 200 V, the low value chips, $\leq 1 \text{ k}\Omega$, were tested in series instead of individually as was the case on the higher resistance values. Once again, new groups of samples were used for each voltage pulse level.



Vishay Thin Film Engineering Test Report

3. Results and Discussion

Table 2 below, is a summary of applied pulse voltage levels and the corresponding minimum and maximum deltas. As the data shows, VTF's thin film PLT product line is minimally affected by periodic pulses, on higher resistance values up to 2 kV, in the 0805 and 1206 case sizes. The smaller case sizes are minimally affected up to 1.2 kV and 1.4 kV on critical and high values. As previously stated, the low value resistors were tested in series. The resultant voltage drop across the resistors is reflected in the reported pulse test voltage levels in table 2. As the data shows, VTF's low value PLT resistors are minimally affected up to 125 V on the 0805 and 1206 case sizes and 50 V for the 0603 case size.

TABLE 2 - SURGE IMMUNITY TEST RESULTS SUMMARY. Table with columns: SAMPLE DESCRIPT., DELTA RES., and PULSE TEST VOLTAGE LEVEL (20, 25, 30, 40, 50, 75, 100, 125, 150, 175, 200, 400, 600, 800, 1000, 1200, 1400, 1600, 1800, 2000). Rows include various resistor types like PLT0603, PLT0805, and PLT1206 with their respective Delta Res. values.

This pulse test data is also presented in graphical format in figures 4 through 7 of appendix A.

TECHNICAL NOTE



Vishay Thin Film Engineering Test Report

4. Conclusion

Based on the results of this work, it can be concluded that VTF's PLT product line is able to withstand high pulse loads, with minimal affect on performance, when tested in accordance to IEC 60115-1 requirements.

Appendix A

VTF PLT Low Value Surge Immunity Results

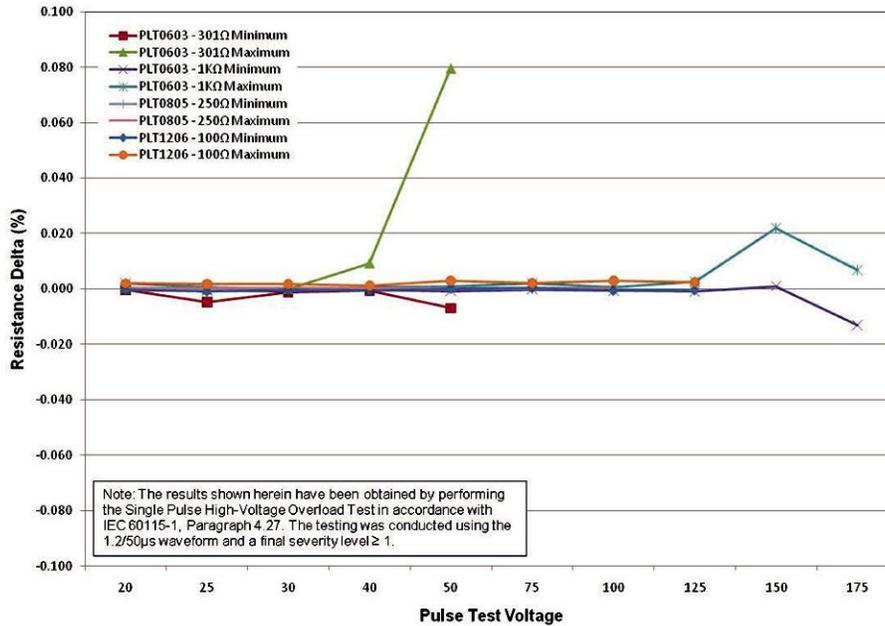


Fig. 4 - Low Value Surge Immunity Test Results

VTF PLT0603 Surge Immunity Test Results

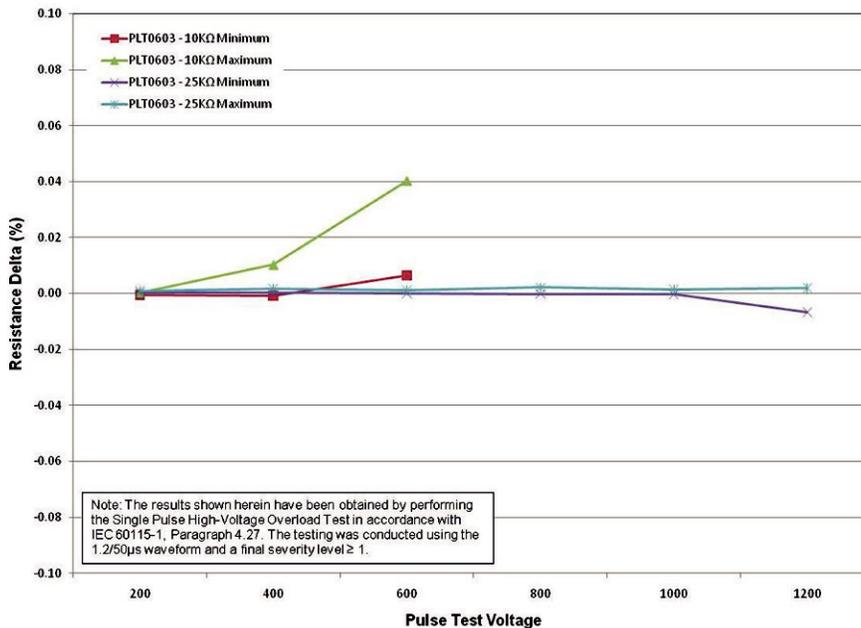


Fig. 5 - 0603 Case Size Surge Immunity Test Results

TECHNICAL NOTE

Vishay Thin Film Engineering Test Report

