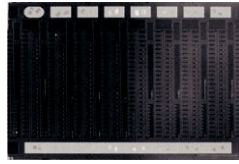
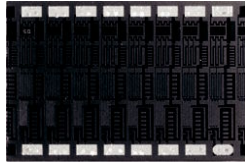




# Wire Bondable Thin Film Eight Resistor Arrays



Product may not be to scale

The CLA and CLB resistor arrays are the hybrid equivalent to the eight resistor common connection and isolated networks available in sips or dips. The resistors are spaced on 0.010" centers resulting in minimal space requirements.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CLA and CLBs are 100 % electrically tested and visually inspected to MIL-STD-883.

### FEATURES

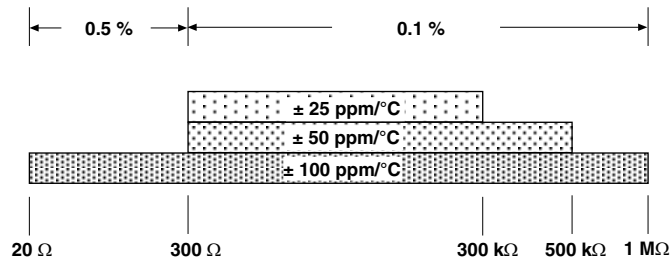
- Wire bondable
- Eight equal value resistors on a 0.060" x 0.090" chip
- Case: 0609
- Resistance range: 20 Ω to 1 MΩ
- Excellent TCR tracking
- Resistor material: Tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Custom values and pad geometries available
- 3 to 12 resistor arrays available
- Moisture resistant

### APPLICATIONS

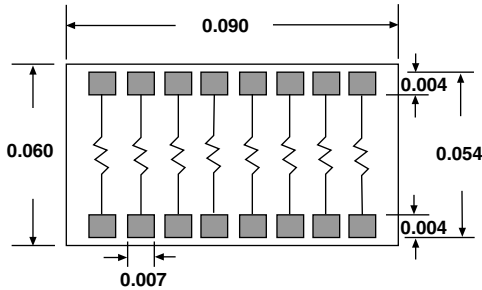
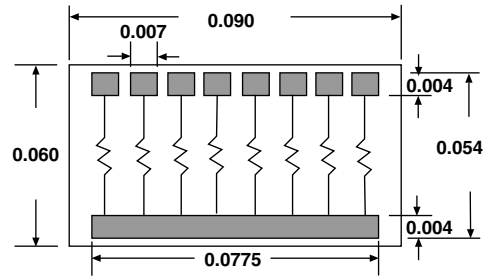
The CLA and CLB thin film resistor arrays are designed for hybrid packages requiring up to eight resistors of the same resistance value and tolerance, as well as excellent TCR tracking. For such hybrids, they afford great savings in cost and space.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES		
PARAMETER	VALUE	UNIT
Total Resistance Range	20 to 1M	Ω
Standard Tolerances	± 0.1, ± 0.5	%
TCR	± 25, ± 50, ± 100	ppm/°C

Tightest Standard Tolerance Available



STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	VALUE	UNIT
TCR Tracking Spread	± 5	ppm/°C
Noise, MIL-STD-202, Method 308 100 Ω to 250 kΩ < 100 Ω or > 251 kΩ	- 35 typ. - 20 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 max. ΔR/R	%
Stability, 1000 h, + 125 °C, 25 mW Absolute Ratio	± 0.25 max. ΔR/R ± 0.05 max. ΔR/R	%
Operating Temperature Range	- 55 to + 125	°C
Thermal Shock, MIL-STD-202 Method 107, Test Condition F	± 0.1 max. ΔR/R	%
High Temperature Exposure, ± 150 °C, 100 h	± 0.2 max. ΔR/R	%
Dielectric Voltage Breakdown	200	V
Insulation Resistance	10 <sup>12</sup> min.	Ω
Operating Voltage	100	V
DC Power Rating at + 70 °C (Derated to Zero at 175 °C)	0.050 per resistor	W
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.1 % max. ΔR/R	%

**DIMENSIONS** in inches

**CLA**

**CLB**

MECHANICAL SPECIFICATIONS	
PARAMETER	
Chip Size	0.060" x 0.090" ± 0.002" (1.50 mm x 2.26 mm ± 0.05 mm)
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO <sub>2</sub>
Resistor Material	Tantalum nitride, self-passivating
Bonding Pads	0.004" x 0.007" (0.10 mm x 0.178 mm)
Number of Top Pads	CLA - 16 CLB - 9
Pad Material	10 kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

GLOBAL PART NUMBER INFORMATION																	
Global Part Number: <b>CLA0830000FFKANHS</b>																	
Global Part Number Description: <b>CLA 8 Res 3K 1%, 100 ppm/°C, Al terminations, no back metal, class H WS</b>																	
<b>C</b>	<b>L</b>	<b>A</b>	<b>0</b>	<b>8</b>	<b>3</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>F</b>	<b>F</b>	<b>K</b>	<b>A</b>	<b>N</b>	<b>H</b>	<b>W</b>	<b>S</b>
MODEL	TYPE	RESISTORS	RES.	RES. MULTIPLIER CODE	TOL. CODE	RATIO TOL.	TCR (ppm/°C)	TERM.	BACK METAL	VISUAL CLASS	PACKAGING CODE						
<b>CL</b>	<b>A</b> = Isolated <b>B</b> = Bussed	<b>03</b> <b>04</b> <b>05</b> <b>06</b> <b>07</b> <b>08</b> <b>09</b> <b>10</b> <b>11</b> <b>12</b>	First 4 digits are significant figures of resistance	<b>B</b> = 0.01 <b>A</b> = 0.1 <b>0</b> = 1 <b>1</b> = 10 <b>2</b> = 100 <b>3</b> = 1000	<b>B</b> = 0.1 % <b>C</b> = 0.25 % <b>D</b> = 0.5 % <b>F</b> = 1.0 % <b>G</b> = 2.0 % <b>J</b> = 5.0 % <b>K</b> = 10.0 %	<b>B</b> = 0.1 % <b>F</b> = 1.0 % <b>N</b> = None	<b>E</b> = ± 25 <b>C</b> = ± 50 <b>K</b> = ± 100 <b>M</b> = ± 250	<b>G</b> = Au <b>A</b> = Al	<b>G</b> = Au <b>N</b> = None	<b>H</b> = Class H <b>K</b> = Class K	<b>WS</b> = Waffle pack, 100 min, 1 mult						



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