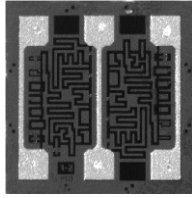


Nichrome Thin Film, Center Tapped Resistors



Product may not be to scale

FEATURES

- Wire bondable
- Center tap feature
- Chip size: 0.030 inches square
- Resistance range total: 10 Ω to 1 MΩ
- Ratio tolerances to: 0.1 %
- Resistor material: Nichrome
- Oxidized silicon substrate for good power dissipation

The CTN series is a center tapped nichrome resistor chip providing excellent stability at 250 mW power levels. The CTN offers the designer flexibility in use as either a single value resistor or as two resistors with a center tap feature. The CTNs six bonding pads allows the user increased layout flexibility.

The CTNs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTNs are 100 % electrically tested and visually inspected to MIL-STD-883.

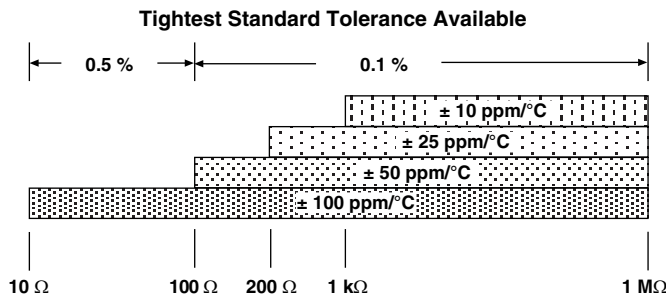
APPLICATIONS

The CTN center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, high power and tracking between two resistors is critical.

Recommended for Hermetic environment where die is not exposed to moisture.

For low values, the resistance of the six bonding-pad configurations can vary, depending on the method of measurement used. Vishay EFI measures low-value resistors by the four wire Kelvin technique.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



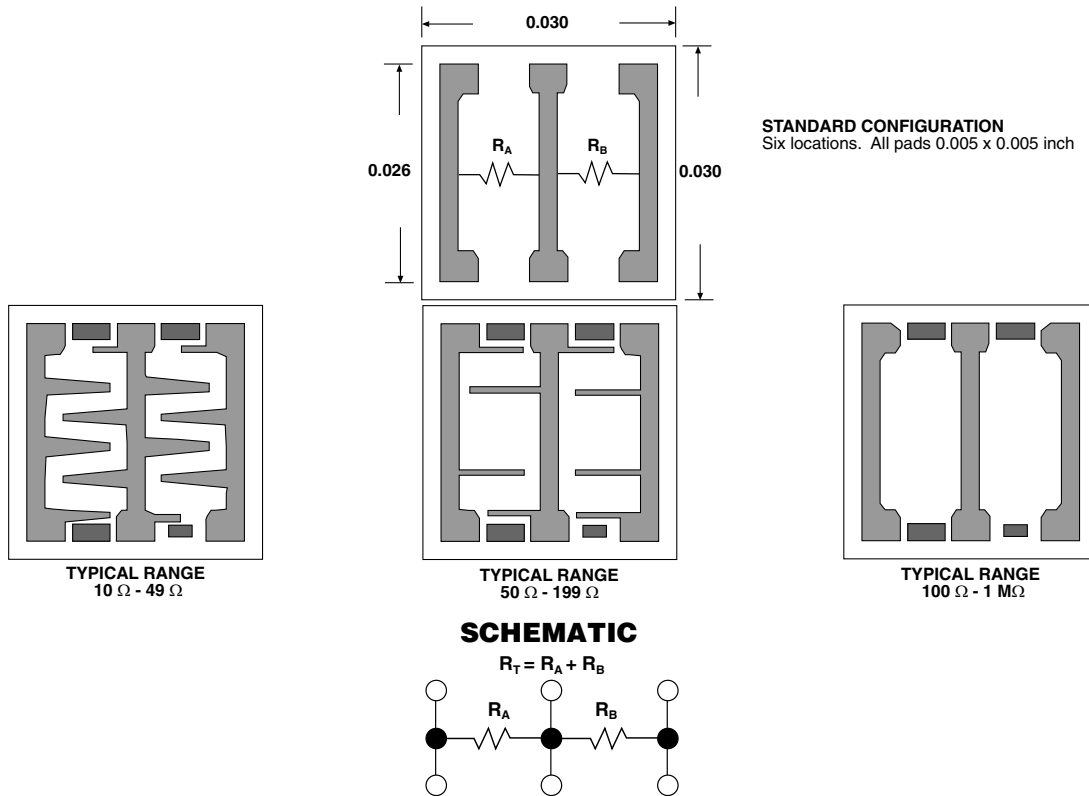
PROCESS CODE	
CLASS H*	CLASS K*
203	263
202	262
200	260
201	261

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR Tracking Between Halves (R_A/R_B)	± 2 ppm/°C *
Center Tap Ratio, R_A/R_B Tolerance	1 ± 1 % standard
Noise, MIL-STD-202, Method 308, 100 Ω - 250 kΩ	- 35 dB typ.
Stability, 1000 h, + 125 °C, 125 mW	± 0.1 % $\Delta R/R$
Operating Temperature Range	- 55 °C to + 125 °C
Dielectric Voltage Breakdown	200 V
Insulation Resistance	10^{12} min.
Operating Voltage	100 V max.
DC Power Rating at + 70 °C (Derated to Zero at + 175 °C)	250 mW

* 20 ppm/°C for $R < 20$

CONFIGURATIONS in inches


MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.05 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Nichrome
Bonding Pad Size	0.005 x 0.005 (0.127 x 0.127 mm) minimum
Number of Pads	6
Pad Material	15 kÅ minimum gold standard
Backing	None, lapped semiconductor silicon

Options: Alphanumeric part marking, up to six characters
 Gold backing for eutectic die attach
 Center tap ratio tolerances to 0.01 %
 Consult Applications Engineer

ORDERING INFORMATION					
Example: 100 % visual, 10 kΩ, ± 1 %, ± 100 ppm/°C TCR, gold pads, class H visual inspection					
W INSPECTION/ PACKAGING	CTN PRODUCT FAMILY	201 PROCESS CODE	1000 RESISTANCE VALUE	1 MULTIPLIER CODE	F TOLERANCE CODE
W = 100 % visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrixtrays (4 % AQL)		See Process Code table	Use first 4 significant digits of resistance (R _T)	C = 0.001 B = 0.01 A = 0.1 0 = 1 1 = 10 2 = 100 3 = 1000 4 = 10 000	B = 0.1 % C = 0.2 % D = 0.5 % F = 1.0 % G = 2.0 % H = 2.5 % J = 5.0 % K = 10 %



Disclaimer

All product specifications and data are subject to change without notice.

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