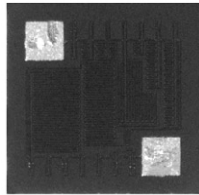


## NiCr Thin Film, Top-Contact Resistor



Product may not be to scale

### FEATURES

- Wire bondable
- Chip size: 20 inches square
- Resistance range: 10 Ω to 510 kΩ
- Resistor material: Nichrome
- Oxidized silicon substrate
- 250 mW power

The SFN series resistor chips offer a combination of nichrome stability, good power rating and small size.

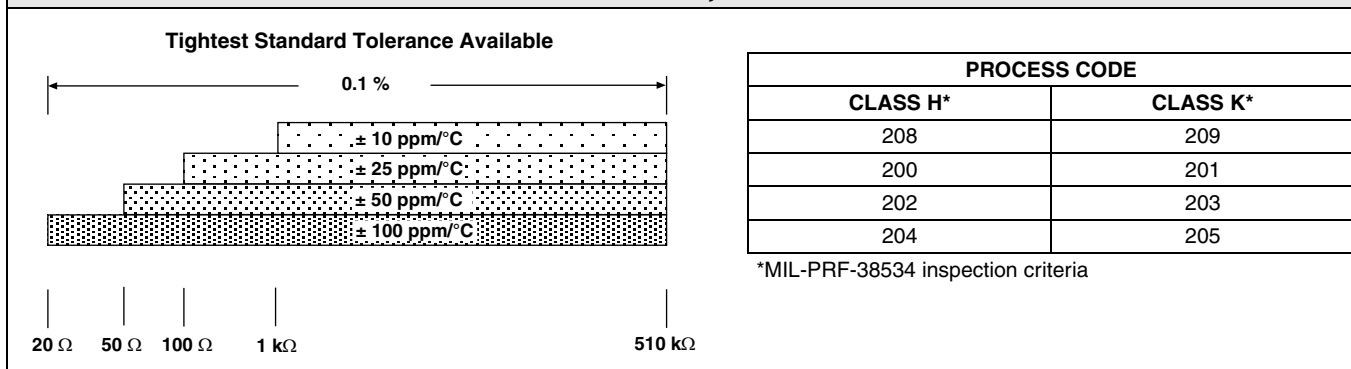
The SFNs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SFNs are 100 % electrically tested and visually inspected to MIL-STD-883.

### APPLICATIONS

Vishay EFI SFN resistor chips are widely used in hybrid packages where space is limited. Designed with capacity to handle substantial power loads, they also have the benefit of nichrome stability.

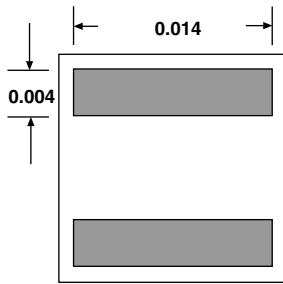
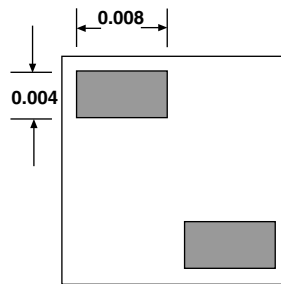
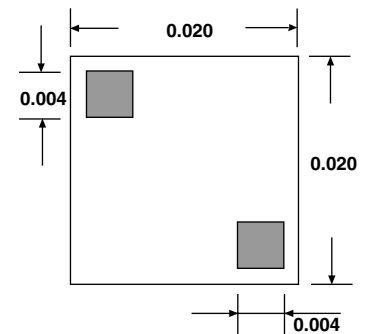
Recommended for hermetic environments where die is not exposed to moisture.

### TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



### STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100 Ω - 250 kΩ < 100 Ω or > 251 kΩ	- 35 dB typ. - 20 dB typ.
Stability, 1000 h, + 125 °C, 50 mW	± 0.25 % max. ΔR/R
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 % max. ΔR/R
High Temperature Exposure, + 150 °C, 100 h	± 0.5 % max. ΔR/R
Dielectric Voltage Breakdown	200 V
Insulation Resistance	10 <sup>12</sup> min.
Operating Voltage	100 V max.
DC Power Rating at + 70 °C (Derated to Zero at + 175 °C)	250 mW
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 % max. ΔR/R

**DIMENSIONS** in inches

**TYPICAL RANGE**  
 10 Ω - 55 Ω

**TYPICAL RANGE**  
 56 Ω - 7.4 kΩ

**TYPICAL RANGE**  
 7.5 kΩ - 510 kΩ

**SCHEMATIC**


<b>MECHANICAL SPECIFICATIONS</b> in inches	
PARAMETER	
Chip Size	0.020 x 0.020 ± 0.003 (0.51 x 0.51 ± 0.05 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO <sub>2</sub>
Resistor Material	Nichrome (passivation optional)
Bonding Pad Size	0.004 x 0.004 (0.10 x 0.10 mm)
Number of Pads	2
Pad Material	15 kÅ minimum gold
Backing	None, lapped semiconductor silicon; Au back optional

**Options:** Aluminum pads  
 Passivation (thermal set plastic)  
 Consult Applications Engineer

<b>ORDERING INFORMATION</b>					
Example: 100 % visual, 10 kΩ, ± 1 %, ± 50 ppm/°C TCR, gold pads, class H visual inspection					
<b>W</b>	<b>SFN</b>	<b>202</b>	<b>1000</b>	<b>1</b>	<b>F</b>
INSPECTION/ PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100 % visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4 % AQL)		See Process Code table	Use the first 4 significant digits of the resistance	<b>B</b> = 0.01 <b>A</b> = 0.1 <b>0</b> = 1 <b>1</b> = 10 <b>2</b> = 100 <b>3</b> = 1000 <b>4</b> = 10 000	<b>B</b> = 0.1 % <b>C</b> = 0.2 % <b>D</b> = 0.5 % <b>F</b> = 1.0 % <b>G</b> = 2.0 % <b>H</b> = 2.5 % <b>J</b> = 5.0 % <b>K</b> = 10 %
					*Coating standard



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