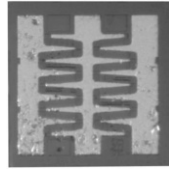
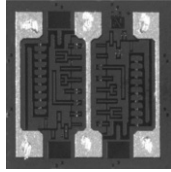


Low Ohmic Value Resistor Supplemental Data Sheet

CHIP RESISTORS



Product may not be to scale

FEATURES

- Wire bondable
- Resistance range total: 1 Ω to 9.9 Ω
- Center Tap
- Chip size: 0.030 inches square
- Oxidized silicon substrate for good power dissipation
- Resistor material: Tantalum nitride, self passivating

The CTR low ohm series provides a center tap option down to 1 ohm for non-critical tolerance applications.

The CTRs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTRs are 100 % electrically tested and visually inspected to MIL-STD-883.

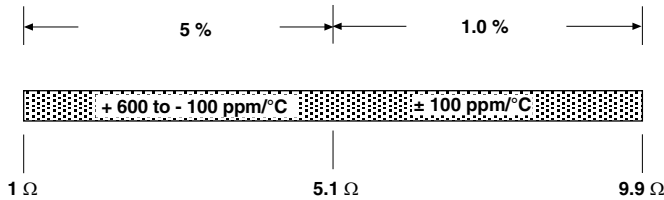
APPLICATIONS

For low values, the resistance of the six bonding pad configurations can vary, depending on the method of measurement used. Vishay EFI measures low value resistors by the four-wire kelvin technique using the method illustrated in the measurement schematic for resistors of less than 10.

Consult Vishay EFI Applications Engineering for alternate measurement method if tighter requirements are needed.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES

Tightest Standard Tolerance Available



PROCESS CODE	
CLASS H*	CLASS K*
101	131

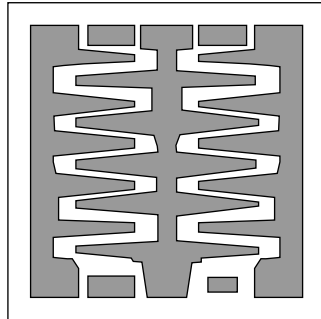
*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

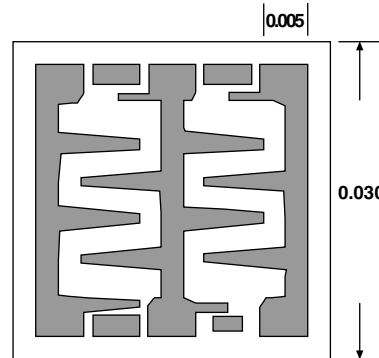
PARAMETER	
TCR Tracking Between Halves (R_A/R_B)	\pm 200 ppm/ $^{\circ}$ C typ.
Voltage Ratio, R_A/R_B : Tolerance	1 \pm 5 %
Noise, MIL-STD-202, Method 308	- 20 dB typ.
Stability, 1000 h, + 125 $^{\circ}$ C, 125 mW	\pm 0.25 % \pm 0.01 % max. $\Delta R/R$
Operating Temperature Range	- 55 $^{\circ}$ C to + 125 $^{\circ}$ C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	\pm 0.1 % max. $\Delta R/R$
High Temperature Exposure, + 150 $^{\circ}$ C, 100 h	\pm 0.2 % + 0.01 % max. $\Delta R/R$
DC Power Rating at + 70 $^{\circ}$ C (Derated to Zero at 175 $^{\circ}$ C)	250 mW
5 x Rated Power Short-Time Overload, + 25 $^{\circ}$ C, 5 s	\pm 0.1 % max. $\Delta R/R$



DIMENSIONS in inches



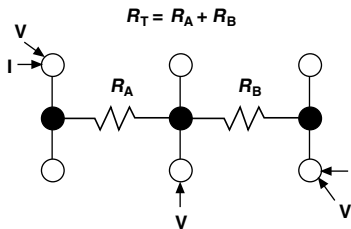
TYPICAL RANGE
1 Ω - 6.7 Ω



TYPICAL RANGE
6.8 Ω - 9.9 Ω

CHIP RESISTORS

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.05 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.005 x 0.005 (0.127 x 0.127 mm) minimum
Number of Pads	6
Pad Material	10 kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

Options: Alphanumeric part parking, up to six character
Gold bonding pads, 15 kÅ minimum;
Contact Applications Engineer

ORDERING INFORMATION					
Example: 100 % visual, 2 Ω, ± 5 %, + 600 to - 100 ppm/°C TCR, aluminum pads, class H visual inspection					
W INSPECTION/ PACKAGING	CTR PRODUCT FAMILY	101 PROCESS CODE	2000 RESISTANCE VALUE	C MULTIPLIER CODE	J TOLERANCE CODE
W = 100 % visually inspected parts X = Sample, visually inspected loaded in matrix trays (4 % AQL)		See Process Code table	Use first 4 significant digits of resistance (R _T)	D = 0.0001 C = 0.001 B = 0.01	F = 1.0 % G = 2.0 % H = 2.5 % J = 5.0 % K = 10 %
					*Coating standard



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