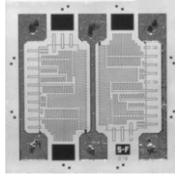


Thin Film Center-Tapped Resistors

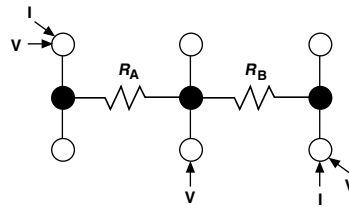


Product may not be to scale

The CTQ series resistor chips offer a wide resistance range with lower shunt capacitance than can be offered with the silicon based resistors but only at a lower power level. The CTQ offers the designer flexibility in use as either a single value resistor or as two resistor with a center tap feature. The CTQs six bonding pads allows the user increased layout flexibility. The CTQs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTQs are 100 % electrically tested and visually inspected to MIL-STD-883.

FEATURES

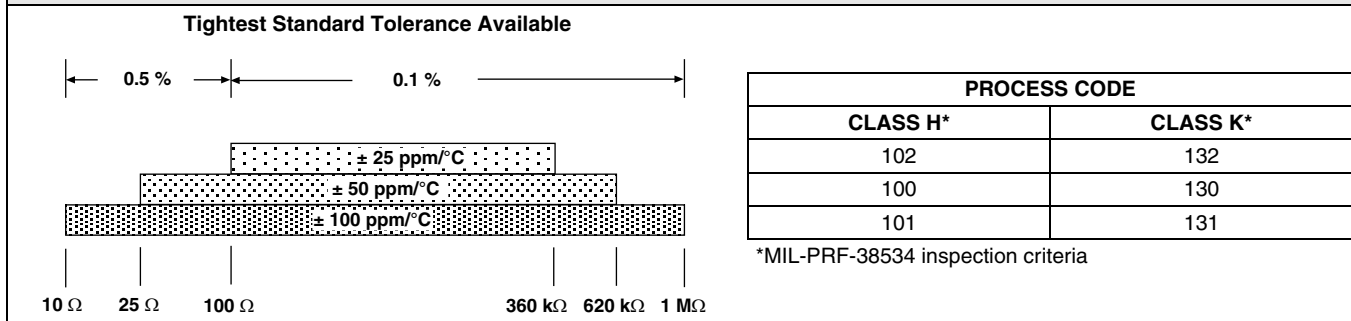
- Wire bondable
- Center tap feature
- Chip size: 0.030 inches square
- Resistance range total: 10 Ω to 1 MΩ
- Resistor material: Tantalum nitride, self-passivating
- Moisture resistant
- Quartz substrate
- Low shunt capacitance < 0.1 pF



APPLICATIONS

The CTQ center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, low shunt capacitance and tracking between two resistors is critical. For low values, the resistance of the six bonding pad configuration can vary, depending on the method of measurement used. Vishay EFI measures low-value resistors by the four-wire kelvin technique.

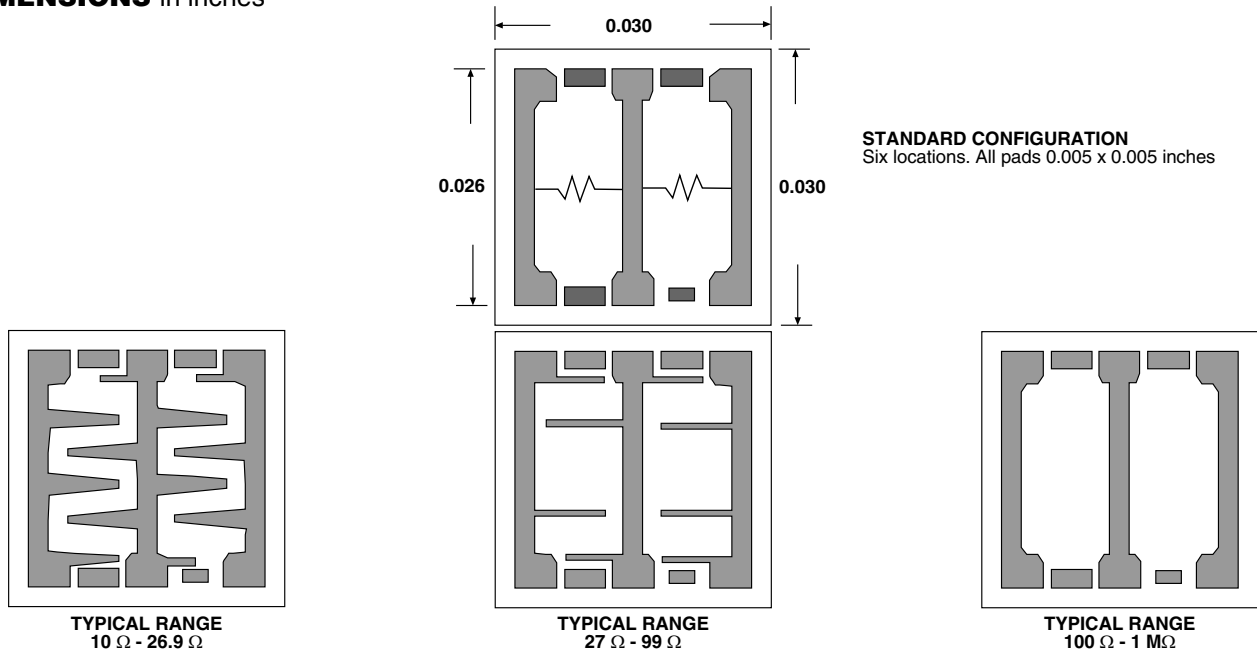
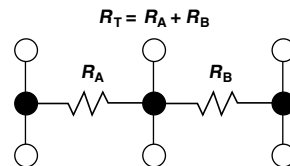
TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR Tracking Between Halves (R_A , R_B)	± 2 ppm/°C*
Center Tap Ratio, R_A/R_B : Tolerance	1 ± 1 % standard
Noise, MIL-STD-202, Method 308, 100 Ω - 250 kΩ < 100 Ω or > 251 kΩ	- 35 dB typ. - 20 db typ.
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 % max. $\Delta R/R$
Stability, 1000 h, + 125 °C, 30 mW	± 0.25 % max. $\Delta R/R$
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 % max. $\Delta R/R$
High Temperature Exposure, + 150 °C, 100 h	± 0.2 % max. $\Delta R/R$
Dielectric Voltage Breakdown	400 V
Insulation Resistance	10^{12} min.
Operating Voltage	200 V
DC Power Rating at + 70 °C (Derated to Zero at + 175 °C)	60 mW
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 % max. $\Delta R/R$ %

*5 ppm/°C for $R < 100$. 20 ppm/°C for $R < 20$

DIMENSIONS in inches

SCHEMATIC


MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.05 mm)
Chip Thickness	0.010 ± 0.003 (0.254 ± 0.05 mm)
Chip Substrate Material	Quartz
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.005 x 0.005 (0.127 x 0.127 mm)
Number of Pads	6
Pad Material	10 kÅ minimum aluminum
Backing	None, lapped quartz

Options: Alphanumeric part marking, up to six characters
 Gold bonding pads, 15k Å minimum
 Center-tap ratio tolerances to 0.05 %
 1 to 10 Ω values available
 Contact Applications Engineer

ORDERING INFORMATION					
Example: 100 % visual, 10 kΩ, ± 1 %, ± 100 ppm/°C TCR, aluminum pads, class H visual inspection					
W INSPECTION/ PACKAGING	CTQ PRODUCT FAMILY	101 PROCESS CODE	1000 RESISTANCE VALUE	1 MULTIPLIER CODE	F TOLERANCE CODE
W = 100 % visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4 % AQL)		See Process Code table	Use first 4 digits significant digits of the resistance (R_T)	D = 0.0001 C = 0.001 B = 0.01 A = 0.1 0 = 1 1 = 10 2 = 100 3 = 1000 4 = 10 000	B = 0.1 % C = 0.2 % D = 0.5 % F = 1.0 % G = 2.0 % H = 2.5 % J = 5.0 % K = 10 %



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