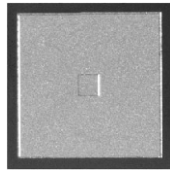


Thin Film Single Value Chip and Wire Capacitors



Product may not
be to scale

The NC series of thin film capacitors has the advantage of increased performance and smaller size when compared with its thick film counterparts. These chips are available in sizes down to 20 mil square and in capacitances up to 1000 pF.

Parts require epoxy or eutectic die attach to substrate and one wire bond.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The NC's are 100 % electrically tested and visually inspected to MIL-STD-883.

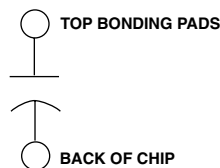
FEATURES

- Wire bondable
- Small size: 0.020 to 0.060 inches square
- Substrate: Silicon with gold backing
- Dielectric: Silicon dioxide/silicon nitride
- Capacitance range: 0.5 pF to 1000 pF

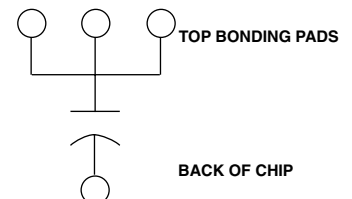
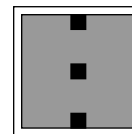
APPLICATIONS

The NC series of capacitor chips are designed for assembly in hybrid circuits using conventional wire-bonding techniques. They provide excellent stability and performance, and their small size gives the hybrid designer greater layout flexibility. They are available as MNOS or MOS capacitors. The MOS version is to be preferred when low dielectric absorption is required.

ELECTRICAL SCHEMATIC NCA/NCB/NCC



ELECTRICAL SCHEMATIC NCD/NCE



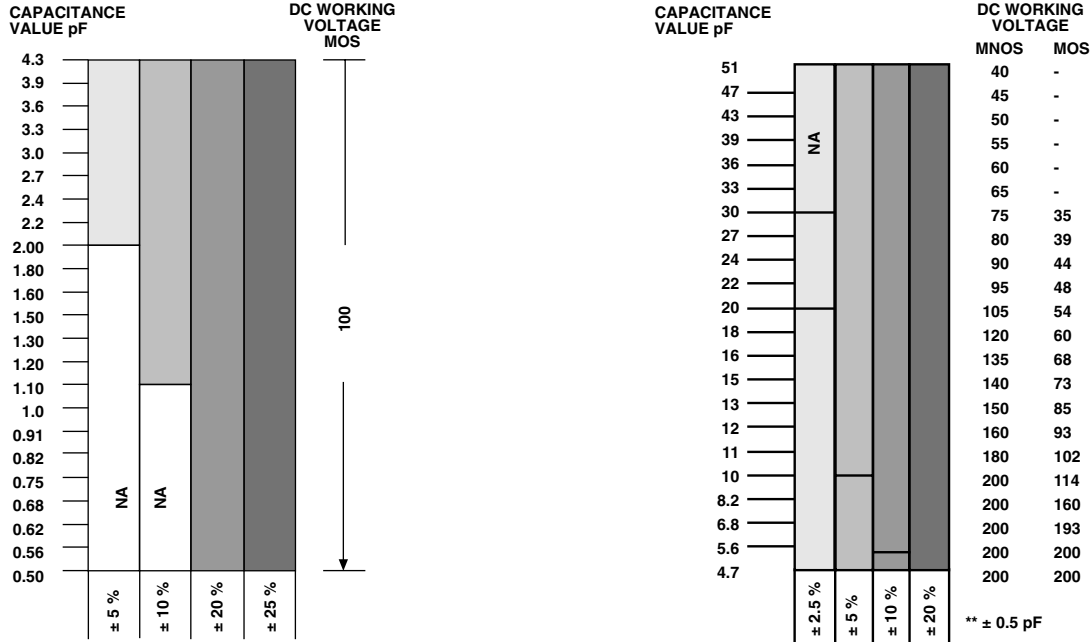
STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
Peak Voltage at + 25 °C	1.5 x working voltage
Dissipation Factor, 1 kHz, 1 V _{RMS} , + 25 °C	0.05 % MNOS 0.1 % MOS
Q at 1 mHz, 50 mV _{RMS} , + 25 °C	1000 min.
TCC, - 55 °C to + 150 °C	+ 45 ± 25 ppm/°C MNOS + 15 ± 25 ppm/°C MOS
Insulation Resistance at Working Voltage, + 25 °C	10 ⁹ min.
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock	± 0.25 % + 0.25 pF max. ΔC/C
Moisture Resistance, MIL-STD-202, Method 106	± 1.0 % + 0.25 pF max. ΔC/C
Short Time Overload, + 25 °C, 5 s, 1.5 x Working Voltage	± 0.25 % + 0.25 pF max.m
High Temperature Exposure, 100 h at 150 °C Ambient	± 0.25 % + 0.25 pF max. ΔC/C
Life, MIL-STD-202, Method 108 Condition D, + 125 °C Ambient, 100 h at Working Voltage	± 0.25 % + 0.25 pF max. ΔC/C



DC WORKING VOLTAGES VALUES AND TOLERANCES

NCA 0.020 inches square

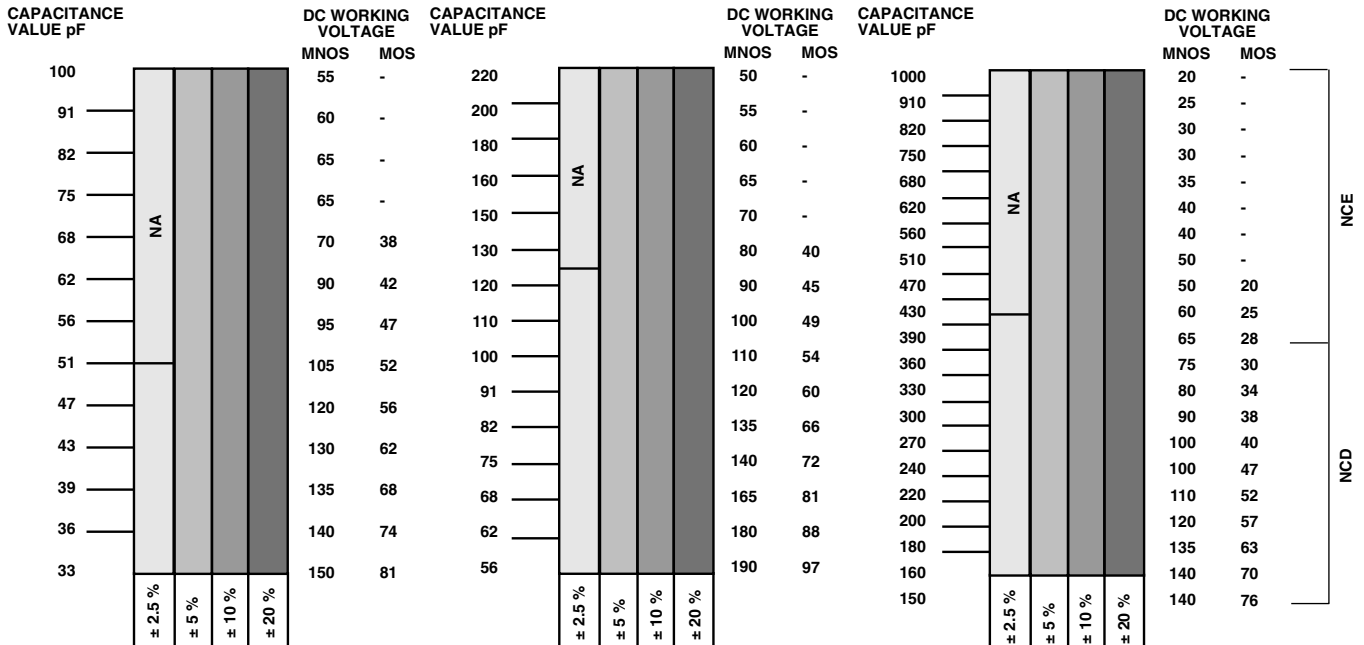
CHIP CAPACITORS



NCB 0.030 inches square

NCC 0.040 inches square

NCD 0.055 inches square NCE 0.060 inches square



DIMENSIONS

0.5 pF - 1.3 pF



1.4 pF - 3.9 pF



4 pF - 9.1 pF



10 pF - 51 pF



NCA
0.020 ± 0.003 inches square

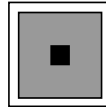
33 pF - 100 pF



NCB

0.030 ± 0.003 inches square

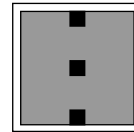
56 pF - 220 pF



NCC

0.040 ± 0.003 inches square

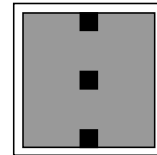
150 pF - 510 pF



NCD

0.055 ± 0.003 inches square

360 pF - 1000 pF



NCE

0.060 ± 0.003 inches square

MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip Size	Per diagrams
Chip Thickness	0.010 ± 0.002 (0.25 ± 0.05 mm)
Chip Substrate Material	Semiconductor silicon
Dielectric	Silicon dioxide/silicon nitride
Bond Pad	0.005 x 0.005 minimum, 10 kÅ aluminum
Backing	3 kÅ minimum gold

Options: Gold bond pads 15 kÅ
Lower profile version is available, consult Applications Engineer

ORDERING INFORMATION

Example: 100 % visualled, 2 pF, ± 5 %, 20 mil MOS capacitor, aluminum pads, class H visual inspection

W INSPECTION/ PACKAGING	NCA PRODUCT FAMILY	017 PROCESS CODE	2000 CAPACITANCE VALUE (pF)	C MULTIPLIER CODE	J TOLERANCE CODE
W = 100 % visually inspected parts in matrix trays per MIL-STD-883	NCA NCB NCC NCD NCE	017 = MOS aluminum 000 = MNOS aluminum	Use first 4 digits significant digits of capacitance	C = 0.001 B = 0.01 A = 0.1 0 = 1	D = ± 0.5 pF H = ± 2.5 %* J = ± 5.0 % K = ± 10 % M = ± 20 % L = ± 25 % N = ± 50 % * MOS only
X = Sample, commercial visually inspected loaded in matrix trays (4 % AQL)					



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