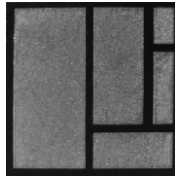
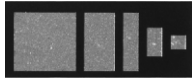


## Thin Film Binary MOS Capacitors



Product may not be to scale

The CBB and CBC MOS capacitor chips each contain five different capacitors in binary increments allowing the user many choices in value selection.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CBB and CBCs are 100 % electrically tested and visually inspected to MIL-STD-883.

**CHIP CAPACITORS**

### FEATURES

- Wire bondable
- User value selection
- Five capacitors on a 0.019 x 0.048 inches (CBB) or 0.044 inches square (CBC) chip
- Capacitance range: 1.0 pF to 93 pF in binary increments
- Dielectric: Silicon dioxide
- Low dielectric loss
- Substrate: Silicon with gold backing

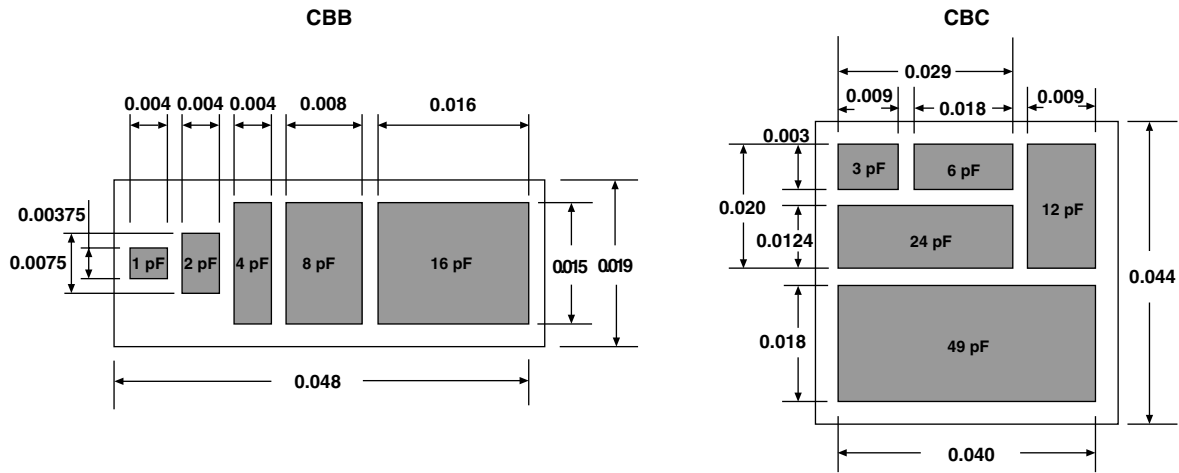
### APPLICATIONS

Vishay EFI CBB and CBC binary MOS multi-value capacitor chips are designed to be a useful device for trimming hybrid circuits by adding or subtracting capacitance, using normal wire-bonding techniques.

<b>WV (DC) VALUES AND TOLERANCES</b>		
CAPACITOR MODEL	CBB	CBC
Total Capacitance	31 pF	93 pF
Individual Capacitance	1 pF, 2 pF, 4 pF, 8 pF, 16 pF	3 pF, 6 pF, 12 pF, 24 pF, 48 pF
Tolerance	± 10 %	± 10 %
DC Working Voltage	75 V	75 V

<b>STANDARD ELECTRICAL SPECIFICATIONS</b>	
PARAMETER	
Peak Voltage at + 25 °C	1.5 x working voltage
Dissipation Factor, 1 kHz, 1 V <sub>RMS</sub> , + 25 °C	0.1 %
Q at 1 mHz, 50 mV <sub>RMS</sub> , + 25 °C	1000 min.
TCC, - 55 °C to + 150 °C	+ 15 ± 25 ppm/°C
Insulation Resistance at Working Voltage, + 25 °C	10 <sup>9</sup> min.
Operating Temperature Range	- 55 °C to + 150 °C
Thermal Shock	± 0.25 % + 0.25 pF max. ΔC/C
Moisture Resistance, MIL-STD-202, Method 106	± 1.0 % + 0.25 pF max. ΔC/C
Short Time Overload, + 25 °C, 5 s; 1.5 x Working Voltage	± 0.25 % + 0.25 pF max. ΔC/C
High Temperature Exposure: 100 h at + 150 °C Ambient	± 0.25 % + 0.25 pF max.
Life, MIL-STD-202, Method 108, Condition D, + 125 °C Ambient, 1000 h at Working Voltage	± 2.0 % + 0.25 pF max. ΔC/C

**CONFIGURATIONS** in inches



**SCHEMATIC**



<b>MECHANICAL SPECIFICATIONS</b> in inches	
PARAMETER	
Chip Size, CBB	0.019 x 0.048 ± 0.002 (0.48 x 1.2 ± 0.05 mm)
CBC	0.044 x 0.044 ± 0.002 (1.1 x 1.1 ± 0.05 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Semiconductor silicon
Dielectric	Silicon dioxide (MOS)
Bonding Pads	10 kÅ minimum aluminum
Backing	3 kÅ minimum gold

**Options:** Gold bonding pads 15 kÅ minimum  
Consult Applications Engineer

<b>ORDERING INFORMATION</b>					
Example: 100 % visualled, 93 pF, 10 %, CBC capacitor, aluminum pads, class H visual inspection					
<b>W</b>	<b>CBC</b>	<b>012</b>	<b>9300</b>	<b>B</b>	<b>K</b>
INSPECTION/ PACKAGING	PRODUCT FAMILY	PROCESS CODE	CAPACITANCE VALUE (pF)	MULTIPLIER CODE	TOLERANCE CODE
W = 100 % visually inspected parts per MIL-STD-883	CBB CBC	<b>008</b> = CBB <b>012</b> = CBC	Use first 4 significant digits of the capacitance (C <sub>T</sub> )	<b>C</b> = 0.001 <b>B</b> = 0.01 <b>A</b> = 0.1 <b>0</b> = 1	<b>J</b> = 5.0 % <b>K</b> = 10 % <b>M</b> = 20 % <b>L</b> = 25 % <b>N</b> = 50 %
X = Sample, visually inspected parts loaded in matrix trays (4 % AQL)					



## Disclaimer

All product specifications and data are subject to change without notice.

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