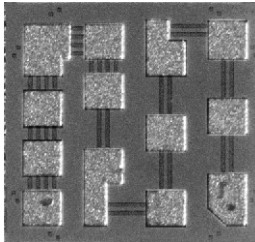


Thin Film Multi-Tap Resistors



Product may not
be to scale

The MTR multi-tap resistors, available in two formats, offer eleven taps allowing the user to select specified increments a wide range of values. The desired resistance value is obtained by bonding the wires to the appropriate pads.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MTRs are 100 % electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

The MTR series of multi-tap resistor chips are designed to satisfy the requirements of prototype development and circuit trimming in hybrid packages through selective wire-bonding.

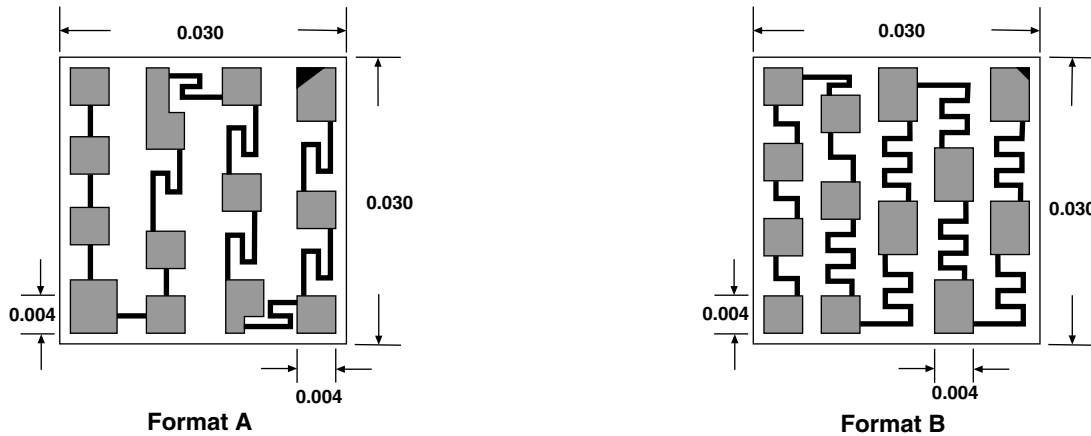
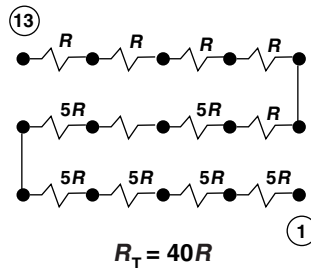
FEATURES

- Wire bondable
- Selectable values by wire bonding
- Chip size: 0.030 inches square
- Standard resistance range: 100 Ω to 24 k Ω or 800 Ω to 240 k Ω
- Resistor material: Tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Ideally suited for hybrid prototyping

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES				
			PROCESS CODE	
			CLASS H*	CLASS K*
Total Resistance Range	Format A Format B	100 Ω , 200 Ω , 400 Ω , 800 Ω , 2.4 k Ω , 8 k Ω , 24 k Ω 800 Ω , 2.4 k Ω , 8 k Ω , 24 k Ω , 80 k Ω , 160 k Ω , 240 k Ω	050 051	060 061
7 Resistors Between Pads 1 and 8 5 Resistors Between Pads 8 and 13		Each 12.5 % of total resistance Each 2.5 % of total resistance	*MIL-PRF-38534 inspection criteria	
Standard Tolerances		± 10 %, ± 20 % of total resistance of all 12 resistors		
TCR		± 100 ppm/ $^{\circ}$ C		

Example: When the total resistance value is 8 k Ω , the resistors between pads 8 and 13 are 200 each, and the resistors between pads 1 and 8 are 1K each.

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
TCR Tracking Between Elements	± 5 ppm/ $^{\circ}$ C
Noise, MIL-STD-202, Method 308	- 30 dB typ.
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 % max. $\Delta R/R$
Stability, 1000 h, + 125 $^{\circ}$ C, 125 mW	± 0.5 % max. $\Delta R/R$
Operating Temperature Range	- 55 $^{\circ}$ C to + 125 $^{\circ}$ C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 % max. $\Delta R/R$
High Temperature Exposure + 150 $^{\circ}$ C, 100 h	± 0.5 % max. $\Delta R/R$
Dielectric Voltage Breakdown	200 V
Insulation Resistance	10^{12} min.
Operating Voltage	100 V max.
DC Power Rating at + 70 $^{\circ}$ C (Derated to Zero at + 175 $^{\circ}$ C)	250 mW, total R
5 x Rated Power Short-Time Overload, + 25 $^{\circ}$ C, 5 s	± 0.25 % max. $\Delta R/R$

DIMENSIONS in inches

SCHEMATIC

MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip Size	0.030 x 0.030 ± 0.003 (0.762 x 0.762 ± 0.076 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Tantalum nitride, self-passivating
Bonding Pads	0.004 x 0.004 (0.10 x 0.10 mm)
Number of Top Pads	13
Pad Material	10 kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

Options: Gold back for eutectic die attach
 Gold bonding pads 15 kÅ minimum thickness
 Other values available on request, consult Application Engineer

ORDERING INFORMATION

Example: 100 % visualled, 8 kΩ, ± 10 %, ± 100 ppm/°C TCR, aluminum pads, format B, class H visual inspection

P/N:	W	MTR	051	8000	0	K
	INSPECTION/ PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
	W = 100 % visually inspected parts in matrix trays per MIL-STD-883		050 = Format A 051 = Format B See Process Code table	Use first 4 significant digits of the resistance (R _T)	A = 0.1 0 = 1 1 = 10 2 = 100	K = 10 % M = 20 % L = 25 % N = 50 %
	X = Sample, commercial visually inspected parts in matrix trays (4 % AQL)					



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