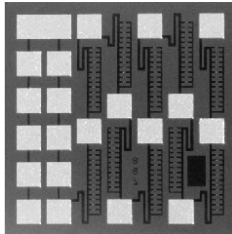


## Thin Film Multi-Tap Resistors



Product may not be to scale

### FEATURES

- Wire bondable
- Selectable values by wire bonding
- Resistance range: 1.1 kΩ to 275 kΩ
- Chip size: 0.038 inches square
- Resistor material tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Ideally suited for hybrid prototyping

The MTT multi-tap resistors offer nineteen taps allowing the user to select specified increments and a wide range of values. The desired resistance value is obtained by bonding the wires to the appropriate pads.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MTT's are 100 % electrically tested and visually inspected to MIL-STD-883.

### APPLICATIONS

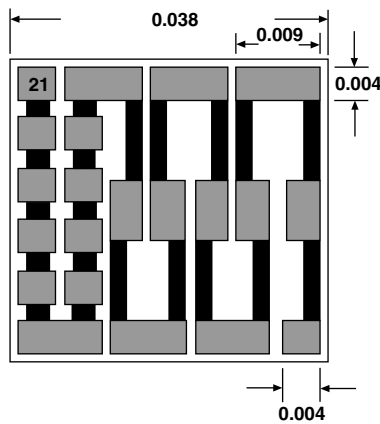
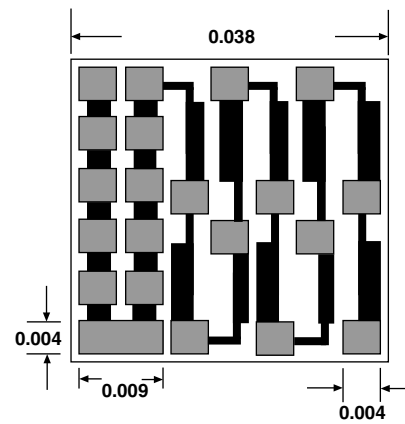
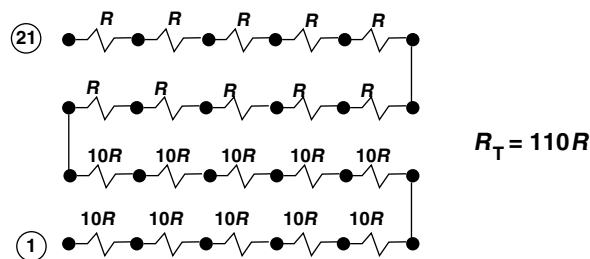
The MTT series of multi-tap resistor chips are designed to satisfy the requirements of prototype development and circuit trimming in hybrid packages through selective wire-bonding.

CHIP RESISTOR ARRAYS

| TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES |  |
|--|--|
| Total Resistance Range                                       | 1.1 kΩ, 2.75 kΩ, 5.5 kΩ, 11 kΩ, 27.5 kΩ, 55 kΩ, 110 kΩ, 275 kΩ       |
| 10 Resistors Between Pads 1 and 11                           | Each 9.1 % of total resistance                                       |
| 10 Resistors Between Pads 11 and 21                          | Each 0.91 % of total resistance                                      |
| Standard Tolerances  | ± 1 %, ± 5 %, ± 10 %, ± 20 % of total resistance of all 20 resistors |
| TCR  | ± 250 ppm/°C   |

**Example:** When the total resistance value is 55 kΩ, the resistors between pads 11 and 21 are 500 Ω each, and the resistors between pads 1 and 11 are 5 kΩ each.

| STANDARD ELECTRICAL SPECIFICATIONS                       |                       |
|--|-----------------------|
| PARAMETER  |                       |
| TCR Tracking Between Elements                            | ± 5 ppm/°C            |
| Noise, MIL-STD-202, Method 308                           | - 30 dB typ.          |
| Moisture Resistance, MIL-STD-202, Method 106             | ± 0.5 % max. ΔR/R     |
| Stability, 1000 h, + 125 °C, 125 mW                      | ± 0.5 % max. ΔR/R     |
| Operating Temperature Range                              | - 55 °C to + 125 °C   |
| Thermal Shock, MIL-STD-202, Method 107, Test Condition F | ± 0.25 % max. ΔR/R    |
| High Temperature Exposure ± 150 °C, 100 h                | ± 0.5 % max. ΔR/R     |
| Dielectric Voltage Breakdown                             | 200 V                 |
| Insulation Resistance                                    | 10 <sup>12</sup> min. |
| Operating Voltage  | 100 V max.            |
| DC Power Rating at + 70 °C (Derated to Zero at + 175 °C) | 250 mW, total R       |
| 5 x Rated Power Short-Time Overload, + 25 °C, 5 s        | ± 0.25 % max. ΔR/R    |

**DIMENSIONS** in inches

**TYPICAL RANGE**  
 1.0 k $\Omega$  - 5.5 k $\Omega$ 

**TYPICAL RANGE**  
 11 k $\Omega$  - 275 k $\Omega$ 
**SCHEMATIC**

**CHIP  
RESISTOR  
ARRAYS**

| <b>MECHANICAL SPECIFICATIONS</b> in inches |  |
|--|--|
| PARAMETER                                  |  |
| Chip Size                                  | 0.038 x 0.038 $\pm$ 0.002 (0.762 x 0.762 mm)               |
| Chip Thickness                             | 0.010 $\pm$ 0.002 (0.254 $\pm$ 0.05 mm)                    |
| Chip Substrate Material                    | Oxidized silicon, 10 k $\text{Å}$ minimum SiO <sub>2</sub> |
| Resistor Material                          | Tantalum nitride, self-passivating                         |
| Bonding Pads                               | 0.004 x 0.004 (0.10 x 0.10 mm)                             |
| Number of Pads                             | 21   |
| Pad Material                               | 10 k $\text{Å}$ minimum aluminum                           |
| Backing                                    | None, lapped semiconductor silicon                         |

**Options:** Gold back for eutectic die attach  
 Gold bonding pads 15 k $\text{Å}$  minimum thickness  
 Other values available on request, consult Application Engineer

| <b>ORDERING INFORMATION</b>   |   |                   |   |  |                                       |  |
|---|---|-------------------|---|--|---------------------------------------|--|
| Example: 100 % visualled, 55 k $\Omega$ , $\pm$ 10 %, $\pm$ 250 ppm/ $^{\circ}$ C TCR, aluminum pads, class H visual inspection |   |                   |   |  |                                       |  |
| <b>P/N:</b>   | <b>W</b>  | <b>MTT</b>        | <b>002</b>  | <b>5500</b>  | <b>1</b>                              | <b>K</b>                                     |
|   | INSPECTION/<br>PACKAGING  | PRODUCT<br>FAMILY | PROCESS<br>CODE   | RESISTANCE<br>VALUE  | MULTIPLIER<br>CODE                    | TOLERANCE<br>CODE                            |
|   | W = 100 % visually inspected<br>parts in matrix trays per<br>MIL-STD-883<br>X = Sample, commercial<br>visually inspected parts in<br>matrix trays ( 4% AQL) |                   | 002 = Class H<br>008 = Class K<br>See Process Code<br>table | Use first 4<br>significant digits of the<br>resistance (R <sub>T</sub> ) | A = 0.1<br>0 = 1<br>1 = 10<br>2 = 100 | K = 10 %<br>M = 20 %<br>L = 25 %<br>N = 50 % |



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