The following guidelines for thin film substrate design are presented to provide the microwave designer with practical and production achievable thin film parameter capabilities as well as to provide a relative cost impact to achieve the tightest specifications. This cost relation is indicated by providing two achievable limits: one with little or no cost premium and the other at some level of cost impact. The tightest tolerances should be specified only where required for circuit performance. If the tightest tolerances are specified for all parameters, even if not required, unnecessary costs will result.

1. **SUBSTRATE SIZE:**
   Sizes are available in most substrate materials to 4 inches x 4 inches. Size tolerances:
   A. Scribe and break ± 0.003 inches most economical
   B. Saw to size ± 0.001 inches small premium
   Surface finish:
   A. 2 - 4 microinches as fired most economical
   B. 2 microinches or 1 microinch maximum polished small premium
   Thickness tolerance as fired:
   A. 0.015 ± 0.002 inches (standard), ± 0.001 inches small premium
   B. 0.010 ± 0.001 inches (standard), ± 0.0005 inches premium
   Thickness tolerance polished:
   A. ± 0.0005 inches standard

2. **METALIZATION:**
   A. Sputtered:
      NiCr, Ta2N, TiW, Ni, Au, Pd, Al,
   B. Electro-Plated:
      Au (to 500 microinches), Ni (to 200 microinches), Cu (to 0.005 inches). (Thick copper can be selectively plated on the power lines).
   Compatibility: While the majority of these materials can be used in multilayer combinations, some combinations are not compatible dependent on patterning requirements.
   For combinations not widely used or when in doubt, please contact Vishay Electro-Films (EFI) application engineering before finalizing specifications.

3. **PATTERNS:**
   A. Minimum Line Widths or Spaces: 0.0005 inches
   B. Line Width Tolerance:
      a. Metal thickness up to 150 microinches ± 0.0001 inches (standard) ± 0.00005 inches (premium)
      b. Metal thickness over 150 microinches ± 0.0001 inches per each 100 microinches thickness:
         Tighter per discussion with Vishay EFI application engineering (premium).
   C. Metalization to Substrate Edge:
      If metalization is brought to the substrate edge, slight disturbance of the metal will occur because of the sawing or scribing operation. If this slight disturbance is not acceptable, a 0.002 inch designed pullback from the edge is required. This also applies to the backside groundplane.

4. **AIR BRIDGES:**
   Width:
   0.001 inch minimum (standard); 0.005 inch (premium); (either true air bridge or over polyimide dielectric).

5. **THROUGH HOLES:**
   A. Diameter:
      0.006 inch minimum
   B. Taper
      The hole will be tapered down from the laser spot entry side, normally the top side, 0.001 inch for every 0.010 inches substrate thickness. The smallest diameter will be used for the hole dimension.
   C. Patterned Metalized Slits:
      Two slits, 0.002 inches wide and 0.006 inches long, will be placed typically 180 °C opposite across the rim of the via. They will not be placed in a signal path unless there is no option

6. **METALIZED THROUGH HOLES:**
   A. Patterns:
      When designing through hole patterns, design a minimum of a 0.005 inches ring around each hole (see figure below) to allow for the tolerance build-up caused by hole placement, manufacturing alignment, diameter tolerance, slight laser entrance hole rounding and other factors.

   If this presents a severe design problem, contact Vishay EFI application engineering.
METALIZED THROUGH HOLES (continued)
B. Double Sided, Front to Back Alignment:
± 0.002 inch (standard), tighter, consult Vishay EFI Application Engineering (premium).
C. Metalization:
The same metalization layers should be used on each side of the substrate when metalized through holes are used. (Plating thickness may be different). For example, if resistor material is required on the top side, it should also be used on the bottom side for the adhesion layer.
D. Size:
Metalized through hole diameters should have a minimum ratio of 0.8 with substrate thickness.

7. FILLED VIAS:
A. Diameter 0.007 inch standard. Center to center hole placement is 0.000015 inch minimum.
Surface finish: The substrate will normally be supplied with a polished or lapped surface necessitated by the fill process.
B. Planarity:
The filled via will not extend above the substrate or be recessed below the substrate by more than 500 microinches.
C. Patterned Metalization Slits:
Two slits, 0.002 inch wide and 0.006 inch long, will be placed typically 180 °C opposite across the rim of the via. They will not be placed in a signal path unless there is no option.

8. RESISTORS
A. Material:
Resistors can be either nichrome or tantalum nitride.
For most microwave applications tantalum nitride is recommended unless unusual tolerances or long term stability requirements exist.
B. Resistivity:
Recommended resistivity for Ta₂N is 25 - 100 Ω/square; for NiCr is 25 - 200 Ω/square.
C. Temperature Coefficient:
a. For Ta₂N, 25 - 50 Ω/square, less than ± 100 ppm/°C; 51 - 100 Ω/square less than ± 150 ppm/°C.
b. For NiCr, 25 - 200 Ω/square, less than ± 50 ppm/°C.
D. Design:
a. Value:
For Ta₂N, Vishay EFI recommends that all resistors be designed to 80 % of value with 20 % trim range (e.g. block resistors, add 20 % to the width.) All high frequency resistors will be laser edge trimmed to value to preserve frequency response (see figure below). However, Vishay EFI can supply resistors of 20 % standard (10 % on demand) or looser tolerance which are designed to 100 % of value with no laser trimming. Matching of identically designed resistors in relatively close proximity, can be held to 3 % without trimming. For nichrome resistors, design all resistors to 80 % of value with a 20 % trim range.

b. Power:
To insure adequate long term stability, the following guidelines should be used relative to power handling (current density).

<table>
<thead>
<tr>
<th>RESISTIVITY (Ω/SQUARE)</th>
<th>CURRENT/0.001 INCH OF LINE WIDTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>4 mA</td>
</tr>
<tr>
<td>50</td>
<td>2 mA</td>
</tr>
<tr>
<td>100</td>
<td>1 mA</td>
</tr>
<tr>
<td>200</td>
<td>0.5 mA</td>
</tr>
</tbody>
</table>

E. Stabilization Temperature:
For the best long term stability, all Ta₂N resistors should be stabilized at approximately 425 °C. However, please note that if nickel has been specified under gold for solderability, temperatures above 350 °C will cause the nickel to diffuse into the the gold creating two problems. One, nickel oxide will form on the gold surface making soldering difficult and secondly, the resistivity of the gold will increase perhaps adversely effecting electrical performance. Specifying palladium in place of nickel will reduce but not eliminate the problem. For most microwave applications where the resistor tolerances are (Ta₂N) 10 % or greater, a stabilization temperature of 350 °C, nominal, should provide adequate long term stability. Remember that if the resistors are designed to 100 % value with no trim allowed, some range in stabilization temperature is required to provide low cost yields. In no case is it recommended that the stabilization temperature be less than 300 °C.