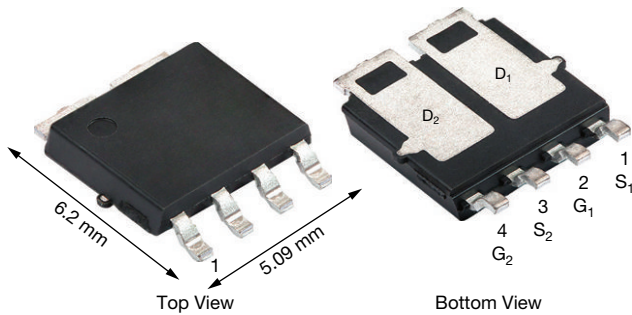




Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L Dual BWL



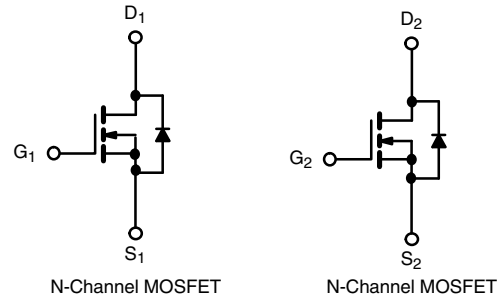
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS COMPLIANT HALOGEN FREE

PRODUCT SUMMARY	
V _{DS} (V)	40
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.006
I _D (A) per leg ^e	85
Configuration	Dual



ORDERING INFORMATION	
Package	PowerPAK® SO-8L
Lead (Pb)-free and halogen-free	SQJ746EP (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current ^e	I _D	T _C = 25 °C ^a	85
		T _C = 125 °C	49
Continuous Source Current (Diode conduction) ^e	I _S	66	A
Pulsed Drain Current ^{b, e}	I _{DM}	134	
Single Pulse Avalanche Current	I _{AS}	L = 0.1 mH	18.5
Single Pulse Avalanche Energy			
Maximum Power Dissipation ^{b, e}	P _D	T _C = 25 °C	80
		T _C = 125 °C	26
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature)		260	

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R _{thJA}	52	°C/W
Junction-to-Case (Drain) ^d	R _{thJC}	1.9	

Notes

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257).
- As per on JESD51-14
- Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system.



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		40	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		2.0	2.8	3.5	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	150	
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	10	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 7\text{ A}$	-	0.0050	0.0060	Ω
		$V_{GS} = 10\text{ V}$	$I_D = 7\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	0.0093	
		$V_{GS} = 10\text{ V}$	$I_D = 7\text{ A}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	0.0112	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 30\text{ A}$		-	70	-	S
Dynamic ^b							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$	-	1014	1420	μF
Output Capacitance	C_{oss}			-	327	458	
Reverse Transfer Capacitance	C_{rss}			-	41	58	
Total Gate Charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}$, $I_D = 5\text{ A}$	-	17	26	nC
Gate-Source Charge ^c	Q_{gs}			-	6	-	
Gate-Drain Charge ^c	Q_{gd}			-	4	-	
Gate Resistance	R_g	f = 1 MHz		2.0	4.1	6.2	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 20\text{ V}$, $R_L = 1.33\text{ }\Omega$ $I_D \cong 15\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$		-	10	15	ns
Rise Time ^c	t_r			-	4	8	
Turn-Off Delay Time ^c	$t_{d(off)}$			-	16	24	
Fall Time ^c	t_f			-	4	8	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I_{SM}			-	-	134	A
Forward Voltage	V_{SD}	$I_F = 7\text{ A}$, $V_{GS} = 0\text{ V}$		-	0.88	1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		-	23	46	ns
Body diode reverse recovery charge	Q_{rr}			-	10	20	nC
Reverse recovery fall time	t_a			-	10	-	ns
Reverse recovery rise time	t_b			-	14	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	-0.8	-	A

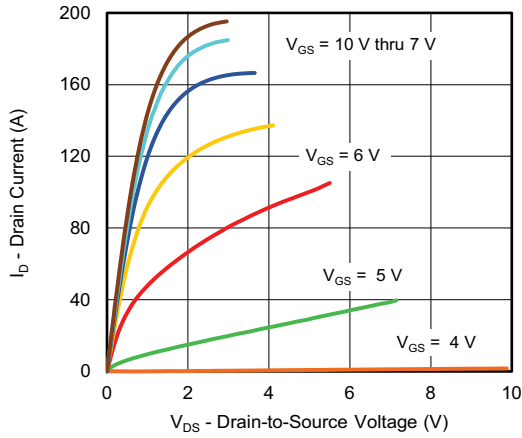
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

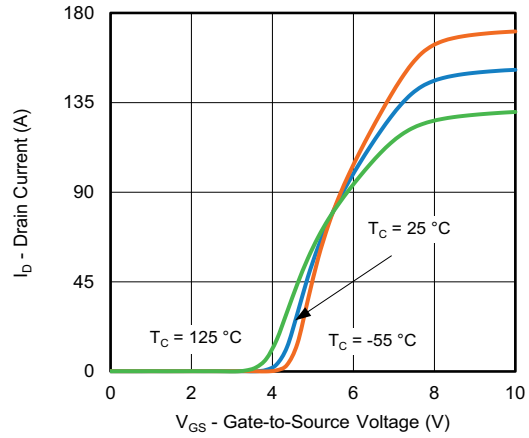
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



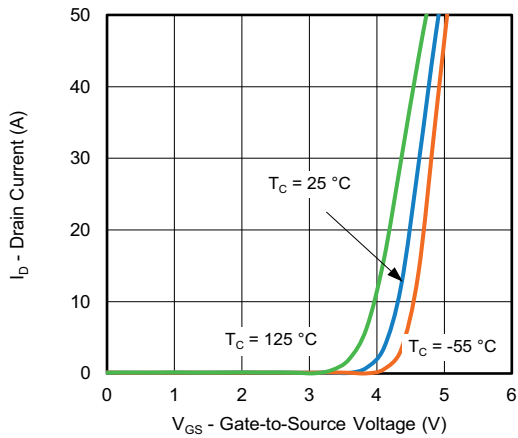
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



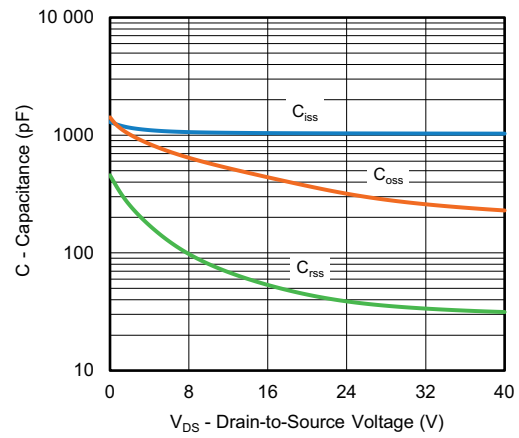
Output Characteristics



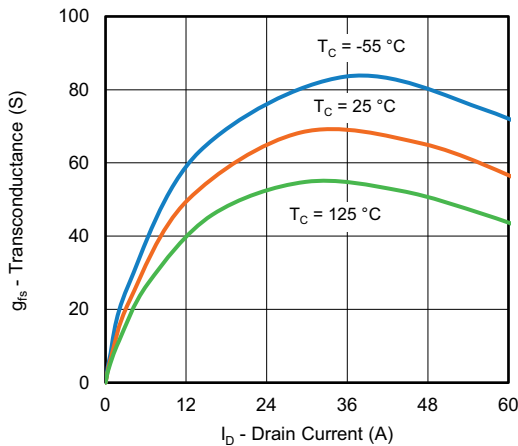
Transfer Characteristics



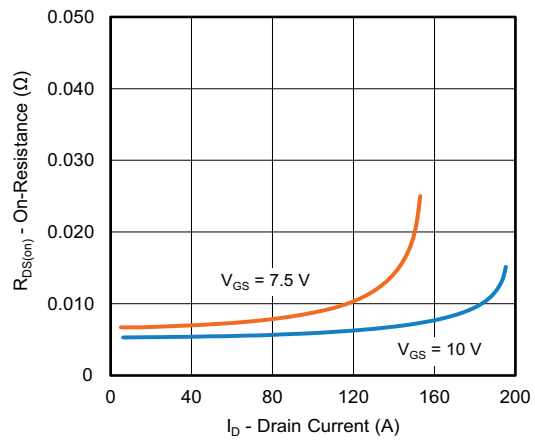
Transfer Characteristics



Capacitance



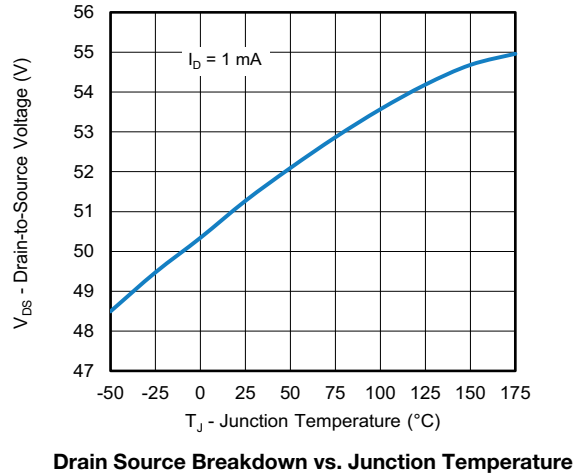
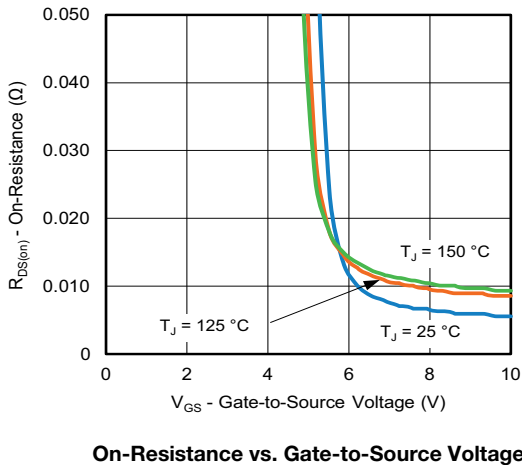
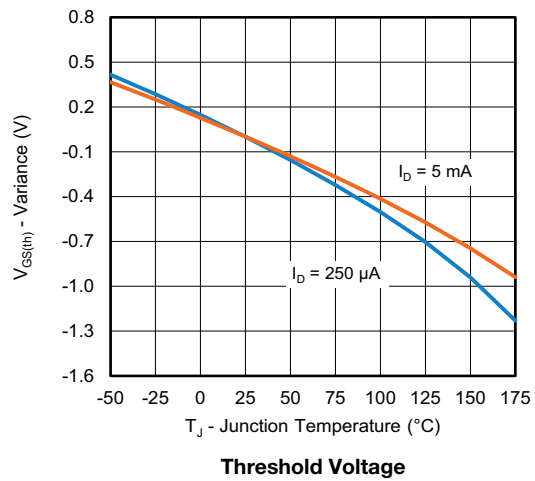
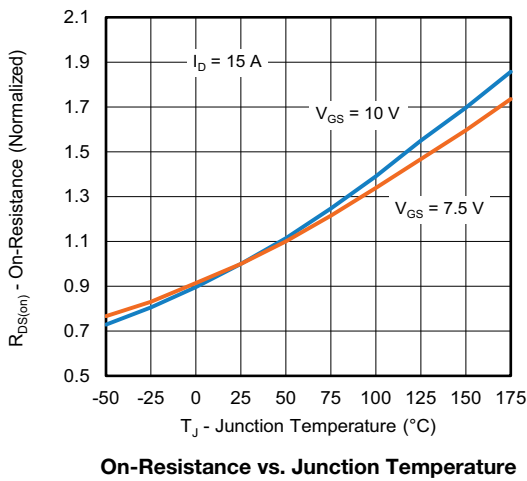
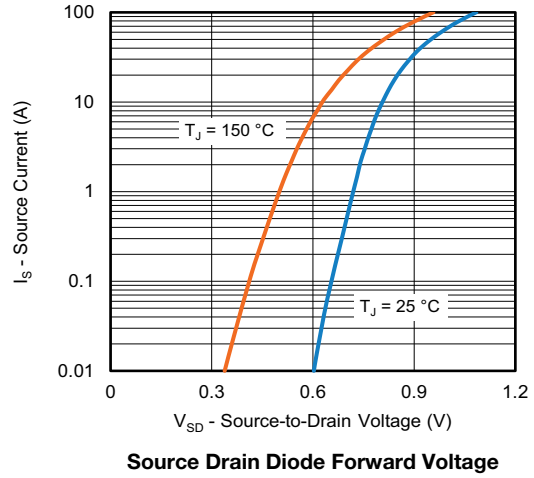
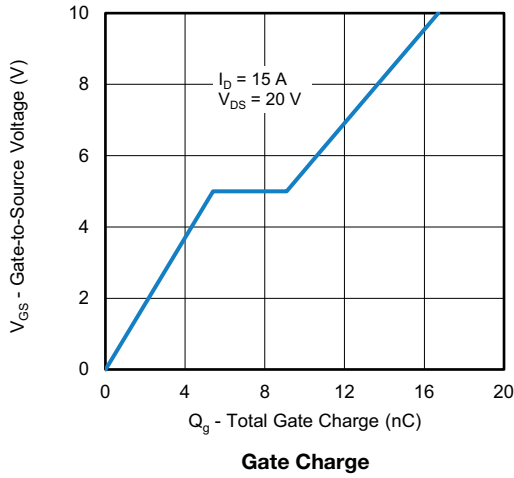
Transconductance



On-Resistance vs. Drain Current

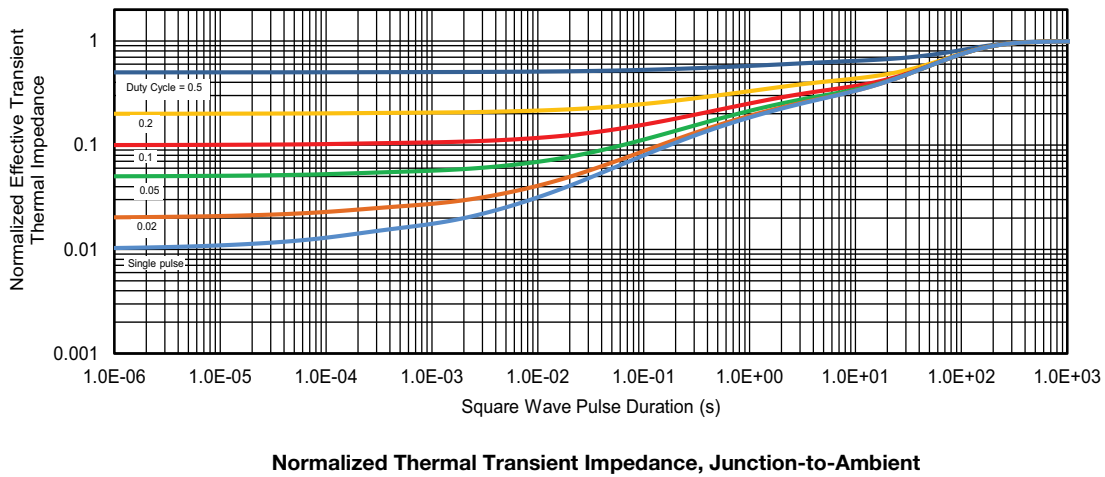
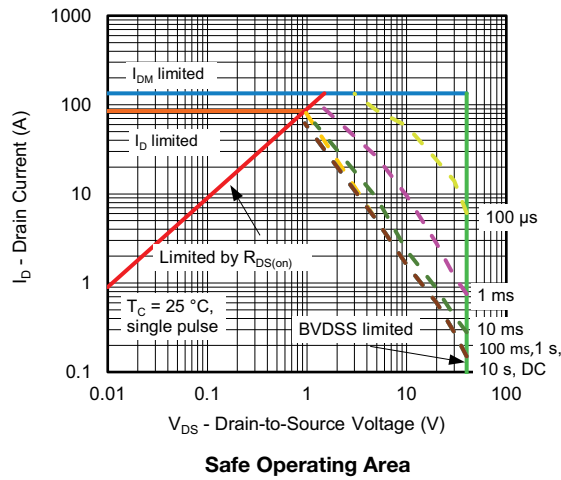


TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



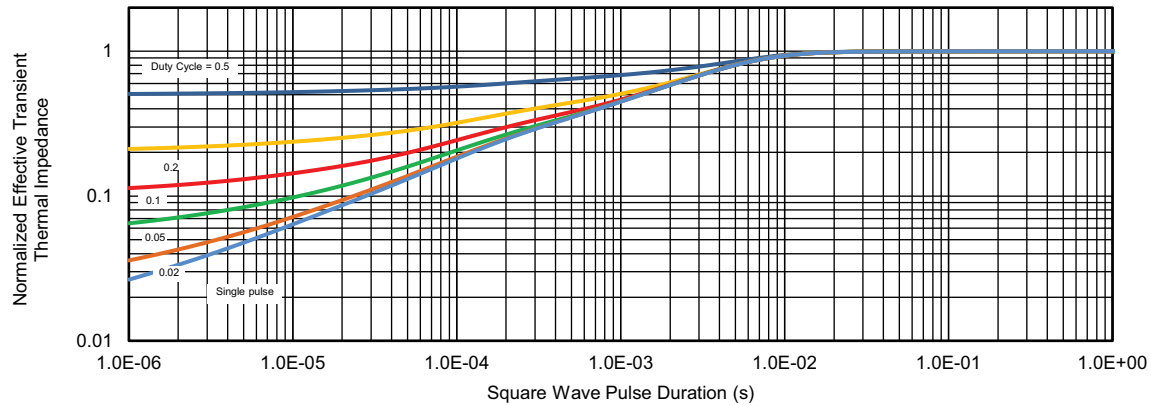


THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)





THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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