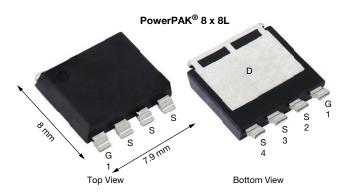
SQJQ116EL

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Vishay Siliconix

Automotive N-Channel 100 V (D-S) 175 °C MOSFET

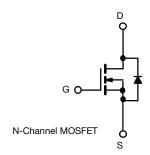


VDS (V) 100 RDS(on) (Ω) at VGS = 10 V 0.0092 RDS(on) (Ω) at VGS = 4.5 V 0.0103 ID (A) e 61 Configuration Single

FEATURES

- TrenchFET[®] Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- Thin 1.9 mm height
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>





ORDERING INFORMATION	
Package	PowerPAK 8 x 8L
Lead (Pb)-free and halogen-free	SQJQ116EL (for detailed order number please see <u>www.vishay.com/doc?79776</u>)

ABSOLUTE MAXIMUM RATING	GS (T _C = 25 °C, unless	s otherwise noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	100	N	
Gate-source voltage		V _{GS}	± 20	V	
Continuous drain current ^e	T _C = 25 °C	- I _D	61		
	T _C = 125 °C		35		
Continuous source current (diode conduction) e		I _S	81	А	
Pulsed drain current ^{a, e}		I _{DM}	212		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	35		
Single pulse avalanche energy		E _{AS}	63	mJ	
Maximum power dissipation ^e	T _C = 25 °C	D	91	W	
	T _C = 125 °C	P _D	30	vv	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) ^c		-	260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount ^b	R _{thJA}	42	°C/W	
Junction-to-case (drain) ^d		R _{thJC}	1.64	0/10	

Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$

b. When mounted on 1" square PCB (FR4 material)

c. See solder profile (www.vishay.com/doc?73257)

e. Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on thermal characteristics of the complete system.

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1 For technical questions, contact: <u>automostechsupport@vishay.com</u> Document Number: 62252

d. As per on JESD51-14

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PARAMETER	SYMBOL	TES	ST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0, I_D = 250 \ \mu A$		100	-	-	v	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$		1.4	1.9	2.5	v	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA	
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 100 V	-	-	1		
		$V_{GS} = 0 V$	$V_{DS} = 100 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$	-	-	50	μA	
		$V_{GS} = 0 V$	$V_{DS} = 100 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	500		
On-state drain current ^a	I _{D(on)}	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	50	-	-	Α	
Drain-source on-state resistance ^a		$V_{GS} = 4.5 V$	I _D = 20 A	-	0.0086	0.0103	- Ω	
	Brach	$V_{GS} = 10 \text{ V}$	I _D = 20 A	-	0.0077	0.0092		
	R _{DS(on)}	$V_{GS} = 10 V$	$I_D = 20 \text{ A}, \text{T}_\text{J} = 125 \ ^\circ\text{C}$	-	-	0.0190		
		$V_{GS} = 10 V$	I _D = 20 A, T _J = 175 °C	-	-	0.0240		
Forward transconductance b	g _{fs}	V _{DS} = 15 V, I _D = 40 A		-	150	-	S	
Dynamic ^b								
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	4670	6538	pF	
Output capacitance	C _{oss}			-	464	650		
Reverse transfer capacitance	C _{rss}			-	29	41		
Total gate charge ^c	Qg		$V_{DS} = 50 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	-	70	105	nC	
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V		-	13	-		
Gate-drain charge ^c	Q _{gd}			-	12	-		
Gate resistance	Rg	f = 1 MHz		0.4	1.0	1.6	Ω	
Turn-on delay time ^c	t _{d(on)}			-	13	20		
Rise time ^c	t _r	$\label{eq:VDD} \begin{array}{l} V_{DD}=50~V,~R_L=2.5~\Omega,\\ I_D\cong20~A,~V_{GEN}=10~V,~R_g=1~\Omega \end{array}$		-	4	8	ns	
Turn-off delay time ^c	t _{d(off)}			-	34	51		
Fall time ^c	t _f			-	6	9		
Source-Drain Diode Ratings and Charac	teristics ^b							
Pulsed current ^a	I _{SM}			-	-	212	Α	
Forward voltage	V _{SD}	$I_{F} = 40 \text{ A}, V_{GS} = 0 \text{ V}$		-	0.7	1.1	V	
Body diode reverse recovery time	t _{rr}	I _F = 15 A, di/dt = 100 A/μs		-	43	86	ns	
Body diode reverse recovery charge	Q _{rr}			-	77	154	nC	
Reverse recovery fall time	ta			-	36	-		
Reverse recovery rise time	t _b			-	7	-	ns	
Body diode peak reverse recovery current	I _{RM(REC)}			-	3.2	-	А	

Notes

a. Pulse test; pulse width $\leq 300~\mu\text{s},$ duty cycle $\leq 2~\%$

b. Guaranteed by design, not subject to production testing

c. Independent of operating temperature

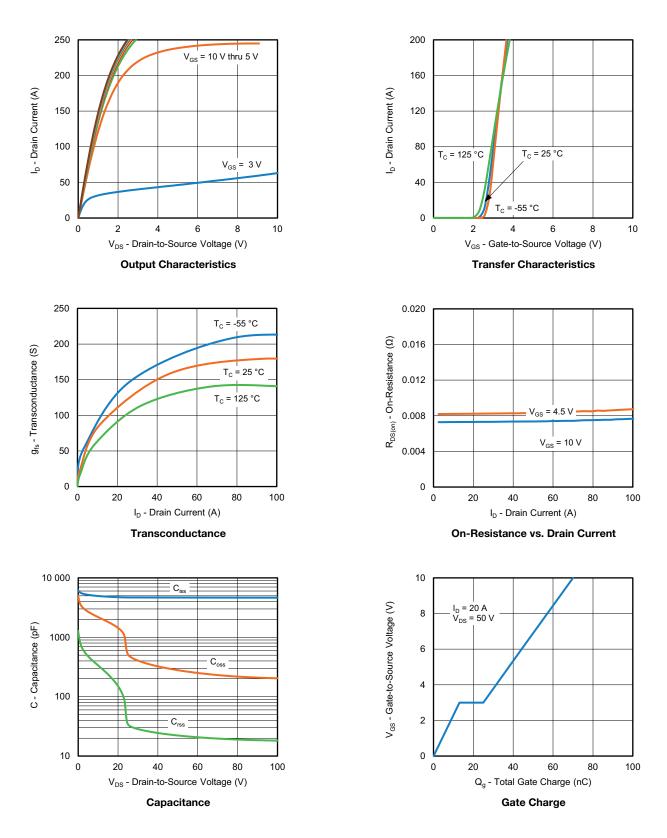
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2



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TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



3

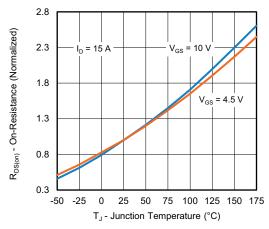
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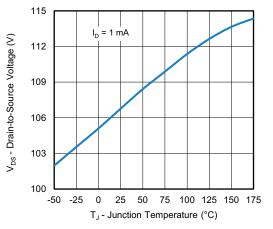
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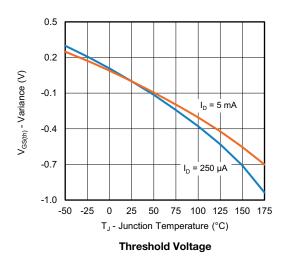
TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)

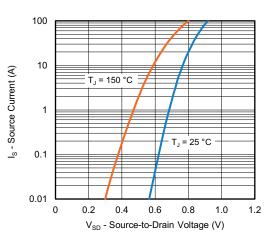


On-Resistance vs. Junction Temperature

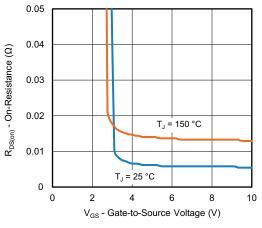


Drain Source Breakdown vs. Junction Temperature

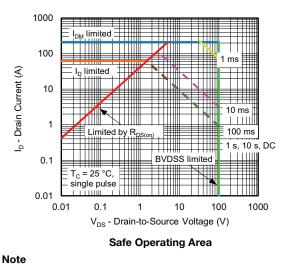




Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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4 For technical questions, contact: <u>automostechsupport@vi</u> Document Number: 62252

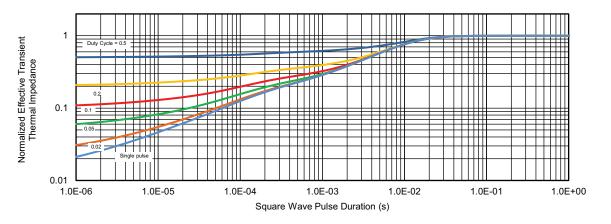
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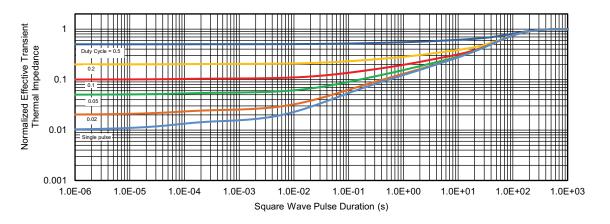
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THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62252.



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