



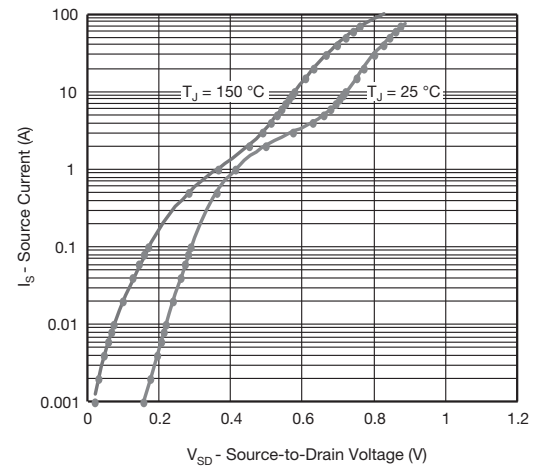
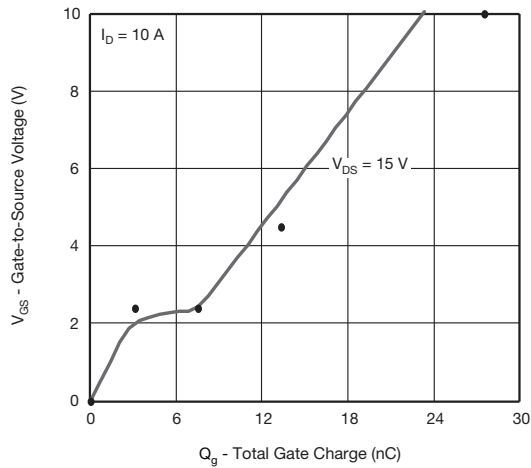
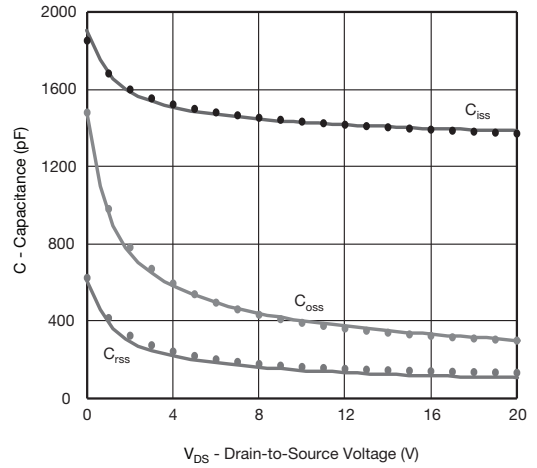
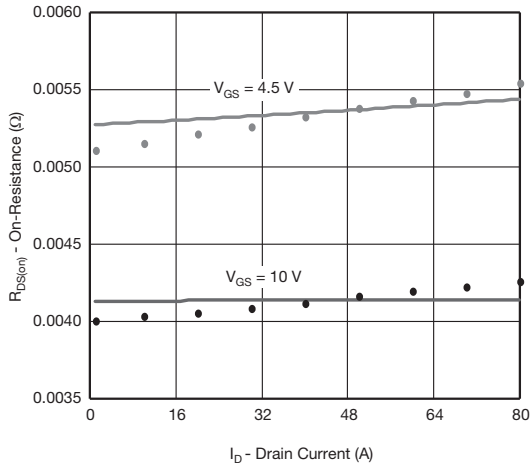
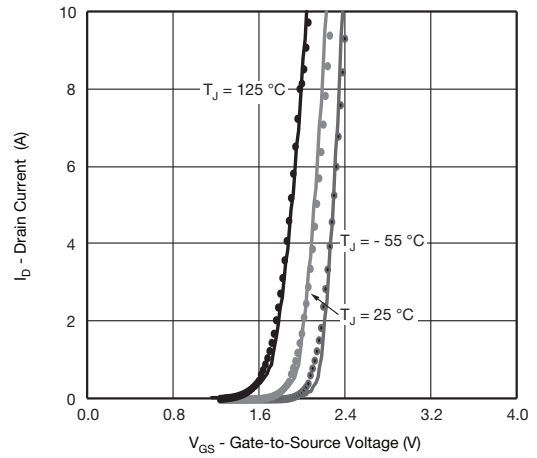
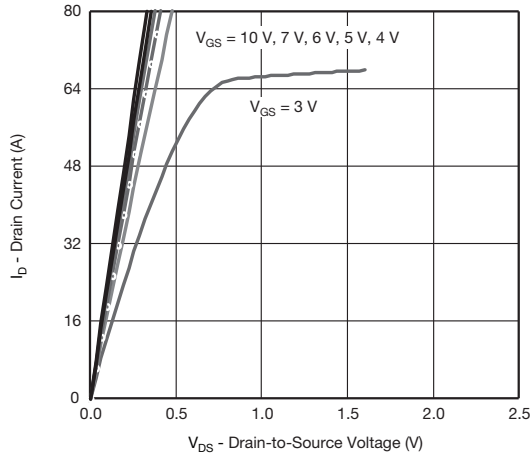
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.3	-	V
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	0.0041	0.0040	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$	0.0052	0.0051	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 10\text{ A}$	52	60	S
Body Diode Voltage	V_{SD}	$I_S = 2\text{ A}$	0.50	0.50	V
Dynamic^b					
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	1400	1390	pF
Output Capacitance	C_{oss}		341	335	
Reverse Transfer Capacitance	C_{rss}		121	145	
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	24	27.5	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	12	13.3	
Gate-Source Charge	Q_{gs}		3.1	3.1	
Gate-Drain Charge	Q_{gd}		4.4	4.4	

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.



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