Quad Channel Monolithic Power Stage

DESCRIPTION

The SiP2204 is a quad channel, fully-integrated monolithic power stage optimized for multi-phase synchronous buck applications. The part has very fast propagation to enable switching frequencies of up to 10 MHz/channel and offers a high power density design for use in applications such as envelope tracking power supplies for RF power amplifiers used in next generation 4G base stations.

Packaged in QFN32 5 x 5, SiP2204 supports input voltages up to 24 V and delivers 500 mA continuous current for each channel.

The SiP2204 incorporates four independent MOSFET gate driver ICs that work with both 3.3 V and 5 V PWM inputs.

FEATURES

- QFN32 5 x 5 package
- Power stage input up to 24 V
- 500 mA per channel continuous current
- 2 A per channel peak current capability
- High frequency operation beyond 5 MHz
- 3.3 V and 5 V PWM logic
- Low PWM propagation delay (typical 13 ns)
- Enable feature to put the output at high impedance when disabled
- Junction temperature: -40 °C to +125 °C

APPLICATIONS

- Envelope tracking (ET) supplies for RF power amplifiers (LDMOS, GaAs FET, GaAs HBT or GaN based)
- Synchronous buck converters

TYPICAL APPLICATION CIRCUIT

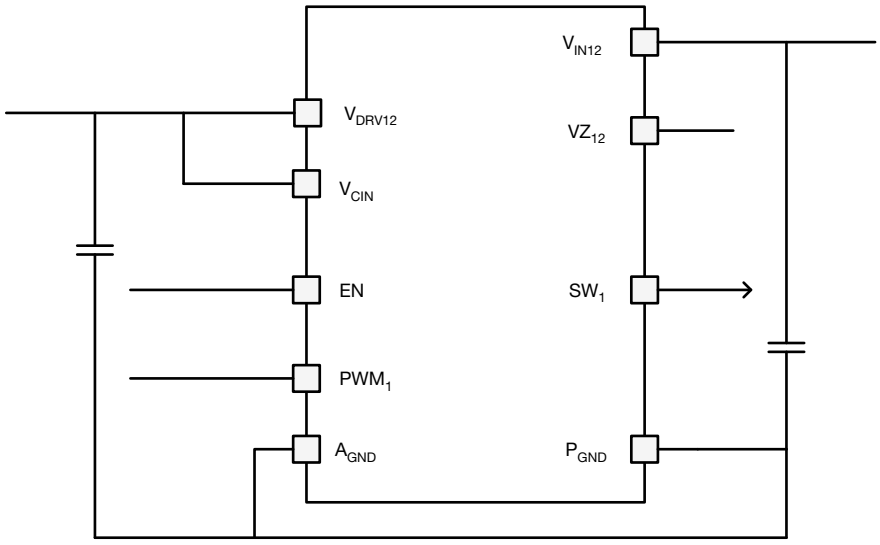
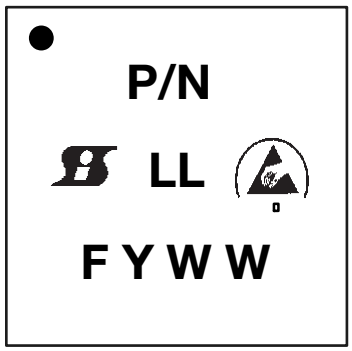


Fig. 1 - Typical Application Circuit for SiP2204 (channel 1 shown)

PART MARKING



●	=	pin 1 indicator
P/N	=	part number code
	=	Siliconix logo
	=	ESD symbol
F	=	assembly factory code
Y	=	year code
WW	=	week code
LL	=	lot code

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL PARAMETER	CONDITIONS	LIMIT	UNIT
Input voltage	V_{INX}	-0.3 to +26	V
Control logic supply voltage	V_{CIN}	-0.3 to +6	
Low-side driver supply voltage	V_{DRVX}	-0.3 to +6	
Switch node (DC voltage)	SW_X	-0.3 to +26	
Switch node (AC voltage) (1)		29	
High-side regulator output monitor voltage	V_{ZX}	(V_{INX} - 6) to V_{INX} and V_{ZX} > -0.3	
All logic inputs and outputs (PWM_X and EN)		-0.3 to V_{CIN} + 0.3	
Max. operating junction temperature	T_J	150	°C
Ambient temperature	T_A	-40 to +125	
Storage temperature	T_{stg}	-65 to +150	
Electrostatic discharge protection	Human body model, JESD22-A114	3000	V
	Charged device model, JESD22-C101	1000	

Notes

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

(1) The specification values indicated “AC” is SW_X to P_{GND}, 29 V (< 50 ns), max.

RECOMMENDED OPERATING RANGE

ELECTRICAL PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
Input voltage (V_{INx})	10	-	24	V
Low-side driver supply voltage (V_{DRVx})	4.5	5	5.5	
Control logic supply voltage (V_{CIN})	4.5	5	5.5	
Thermal resistance from junction to PCB	-	25	-	°C/W
Thermal resistance from junction to case	-	1	-	

PIN CONFIGURATION

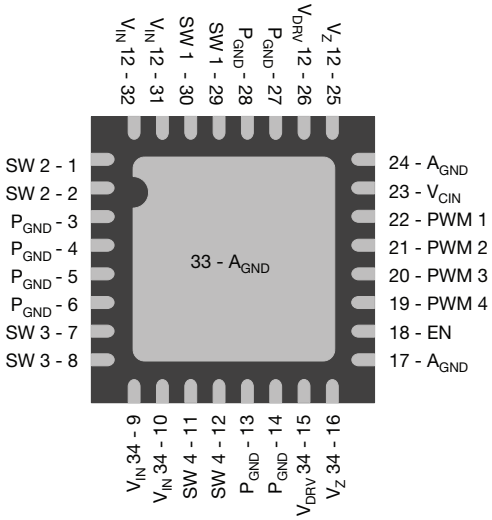


Fig. 2 - Pin Configuration for SiP2204

PIN CONFIGURATION		
PIN NUMBER	**PIN NAME**	**PIN DESCRIPTION**
1, 2	SW 2	Channel 2 driver output
3 to 6, 13, 14, 27, 28	P_{GND}	Low-side driver power return for all channels
7, 8	SW 3	Channel 3 driver output
9, 10	V_{IN} 34	Power stage input voltage and high-side driver power supply for channel 3 and 4
11, 12	SW 4	Channel 4 driver output
15	V_{DRV} 34	Low-side driver power supply for channel 3 and 4
16	V_Z 34	High-side regulator output monitor for channel 3 and 4
18	EN	Global enable pin. Active high
19	PWM 4	Channel 4 PWM input (In phase with SW)
20	PWM 3	Channel 3 PWM input (In phase with SW)
21	PWM 2	Channel 2 PWM input (In phase with SW)
22	PWM 1	Channel 1 PWM input (In phase with SW)
23	V_{CIN}	Supply voltage for internal logic circuitry
17, 24, 33	A_{GND}	Analog ground
25	V_Z 12	High-side regulator output monitor for channel 1 and 2
26	V_{DRV} 12	Low-side driver power supply for channel 1 and 2
29, 30	SW 1	Channel 1 driver output
31, 32	V_{IN} 12	Power stage input voltage and high-side driver power supply for channel 1 and 2

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITION UNLESS OTHERWISE SPECIFIED V_{DRVX} = V_{CIN} = EN = 5 V, V_{INX} = 15 V, V_{INX} - VZ_X = 5 V, no load, PWM rise and fall time = 2 ns T_A = 25 °C for typical value	JUNCTION TEMPERATURE -40 °C to +125 °C unless otherwise specified			UNIT
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Power stage input and high-side driver supply current	I_{VIN}	EN = 0 V, PWM_X = 0 V	-	-	1	µA
		PWM_X = 0 V	-	90	130	
		PWM_X = 3.3 V (80K pull-up on high-side gate)	-	230	330	
		f_{sw} = 4 MHz, D = 10 %, one channel	-	14	27.5	mA
Control logic and low-side driver supply current	I_{VCIN} + I_{VDRV}	EN = 0 V, no switching, PWM = 0	-	-	1	µA
		PWM_X = 0 V (80K pull-down on low-side gate)	-	370	530	
		PWM_X = 3.3 V	-	90	130	
		f_{sw} = 4 MHz, D = 10 %, one channel	-	5	8	mA
PWMx/EN LOGIC (ALSO SEE TIMING DIAGRAM BELOW FOR ILLUSTRATION)						
PWMx/EN rising threshold	V_{TH_R}		2.4	-	-	V
PWMx/EN falling threshold	V_{TH_F}		-	-	0.8	
PWM_X supply current	I_{PWM}	PWM_X = 5 V	-	-	1	µA
EN supply current	I_{EN}	R_{EN} = 1 MΩ to A_{GND}	-	-	8	
PWM on time [1]	t_{PWM_ON}		12	-	-	ns
PWM rising propagation delay	$t_{PD\_R\_PWM}$	From PWM rises to 1.7 V to SW rises to 1.5 V; 25 °C	8	15	22	
		From PWM rises to 1.7 V to SW rises to 1.5 V	-	-	25	
PWM falling propagation delay	$t_{PD\_F\_PWM}$	From PWM falls to 1.7 V to SW falls to 1.5 V; 25 °C	7	18	26	
		From PWM falls to 1.7 V to SW falls to 1.5 V	-	-	30	
PWM propagation delay matching [2]	$t_{PD\_M\_PWM}$	From PWM rises to 1.7 V to SW rises to 1.5 V; 25 °C	-	0.4	0.75	
		From PWM rises to 1.7 V to SW rises to 1.5 V	-	-	1	
EN propagation delay	t_{PD_EN}	From EN rise to V_{CIN} to SW start switching	-	5	-	µs
OUTPUT DRIVER						
Low-side on resistance	$R_{DS(on)\_N}$	I_{sw} = 0.1 A	-	0.35	0.56	Ω
High-side on resistance	$R_{DS(on)\_P}$	I_{sw} = 0.1 A, V_{IN} - V_Z = 5 V	-	0.55	0.92	

Notes

(1) Guaranteed by design

(2) Difference between the maximum and minimum PWM propagation delay among 4 channels

FUNCTIONAL BLOCK DIAGRAM

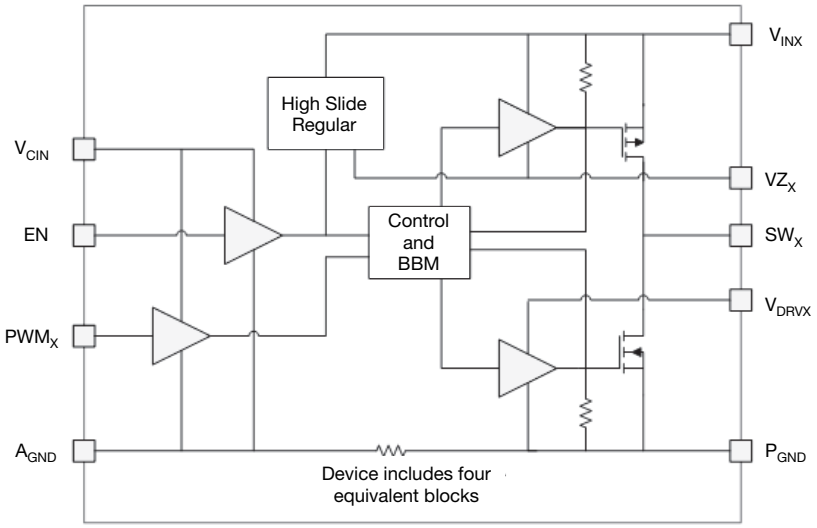


Fig. 3 - Functional Block Diagram for SiP2204

ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING (LINE 2: P/N)**
SiP2204EMP-T1-GE4	QFN32 5 x 5	SiP2204
SiP2204DB	Reference board	

TIMING WAVEFORMS

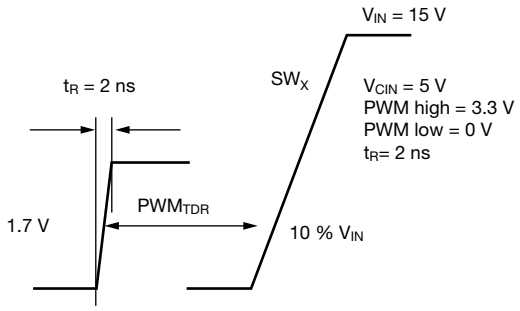


Fig. 4 - Timing Waveform for SiP2204

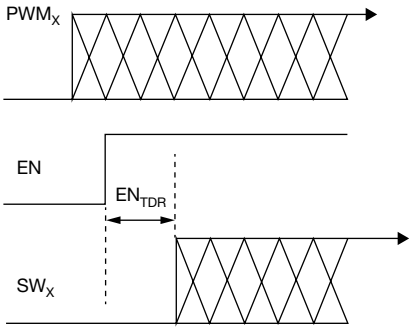


Fig. 5 - Timing Waveform for SiP2204

DETAILED OPERATIONAL DESCRIPTION

PWM Input

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{TH\_PWM\_R}$ the low-side is turned off and the high-side is turned on. When PWM input is driven below $V_{TH\_PWM\_F}$ the high-side turns off and the low-side turns on. The SiP2204 incorporates PWM voltage thresholds that is compatible with 3.3 V and 5 V logic.

Enable (EN)

In the low state, the EN pin shuts down the device. In this state, standby current is minimized. If EN is left unconnected, an internal pull-down resistor will pull the pin to A_{GND} and shuts down the device. The EN pin is a global enable for all four channels when driven above $V_{TH\_EN\_R}$.

High-Side Regulator Output Monitor (V_Z)

V_Z 12 and V_Z 34 are the output monitors for the high-side regulators. V_{ZX} is regulated to 5 V below V_{IN} (typical).

Voltage Input (V_{IN})

The power input to the drain of the high-side power MOSFET and the high-side driver supply. This pin is connected to the high power intermediate BUS rail. An 80 kΩ resistor is connected between the high-side gate and V_{IN}.

Switch Node (SW_X)

The switch node, SW, is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter.

Ground Connections (A_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to A_{GND} (analog ground). The layout of the printed circuit board should be such that the inductance separating the A_{GND} and P_{GND} should be a minimum. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

V_{CIN} is the bias supply for the logic control circuitry of the IC. V_{DRVx} is the bias supply for the low-side gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the logic circuitry.

ELECTRICAL CHARACTERISTICS (V_{OUT} = 2 V, V_{CIN} = V_{DRVx} = 5 V, L = 4.7 µH, unless otherwise noted)

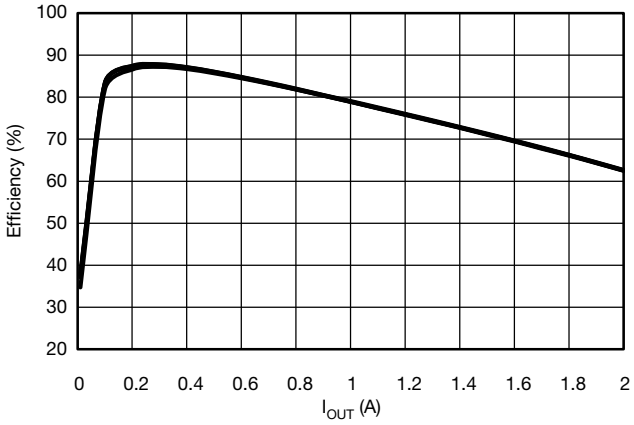


Fig. 6 - Efficiency vs. I_{OUT}
V_{IN} = 8 V, f_{SW} = 1 MHz

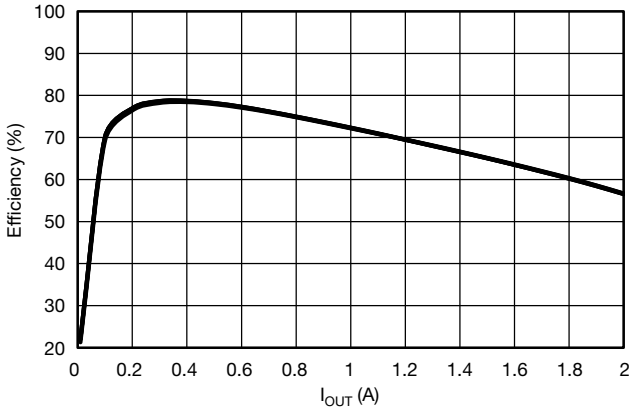


Fig. 7 - Efficiency vs. I_{OUT}
V_{IN} = 8 V, f_{SW} = 5 MHz

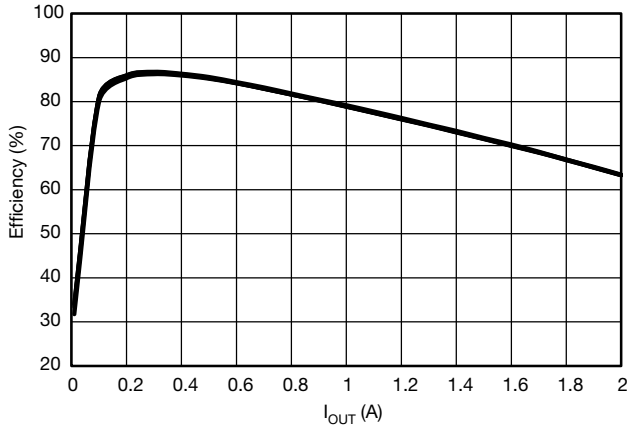


Fig. 8 - Efficiency vs. I_{OUT}
V_{IN} = 10 V, f_{SW} = 1 MHz

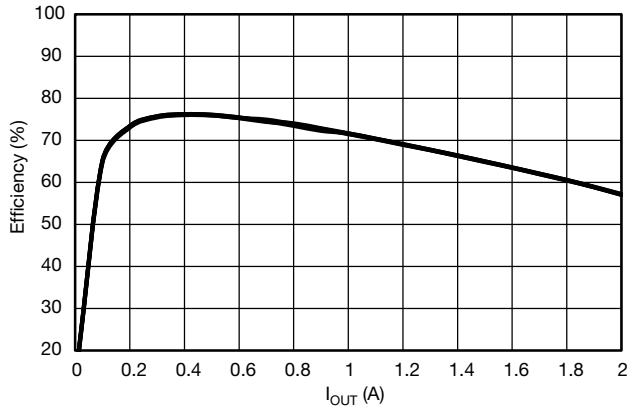


Fig. 9 - Efficiency vs. I_{OUT}
V_{IN} = 10 V, f_{SW} = 5 MHz

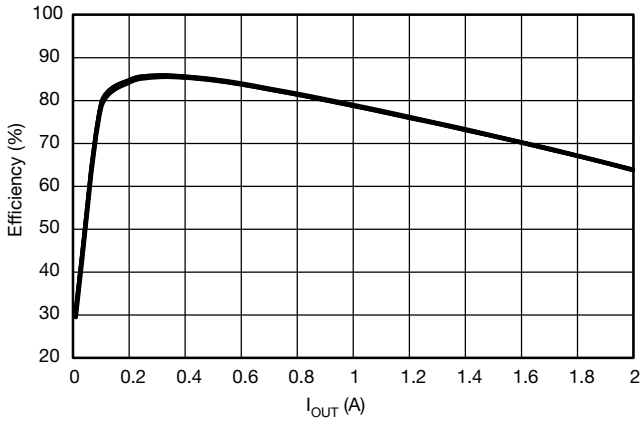


Fig. 10 - Efficiency vs. I_{OUT}
V_{IN} = 12 V, f_{SW} = 1 MHz

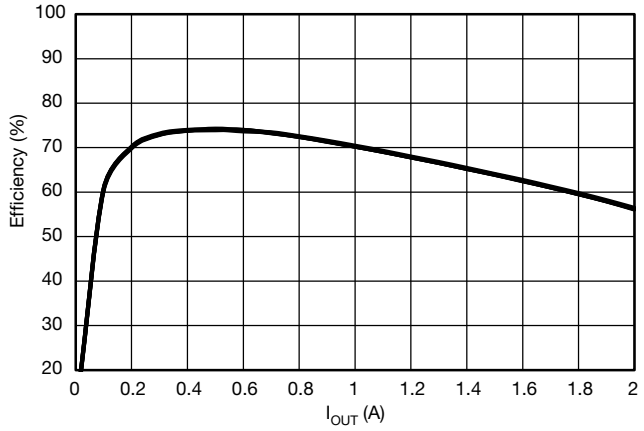


Fig. 11 - Efficiency vs. I_{OUT}
V_{IN} = 12 V, f_{SW} = 5 MHz

ELECTRICAL CHARACTERISTICS (V_{OUT} = 2 V, V_{CIN} = V_{DRVx} = 5 V, L = 4.7 µH, unless otherwise noted)

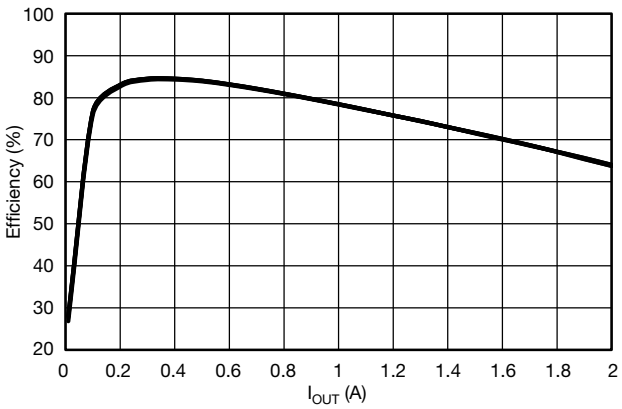


Fig. 12 - Efficiency vs. I_{OUT}
V_{IN} = 15 V, f_{SW} = 1 MHz

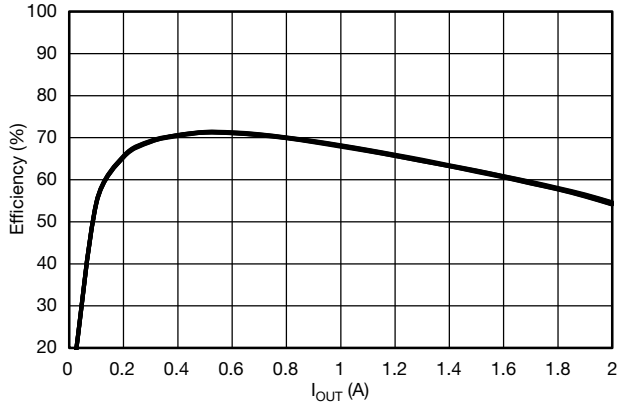


Fig. 13 - Efficiency vs. I_{OUT}
V_{IN} = 15 V, f_{SW} = 5 MHz

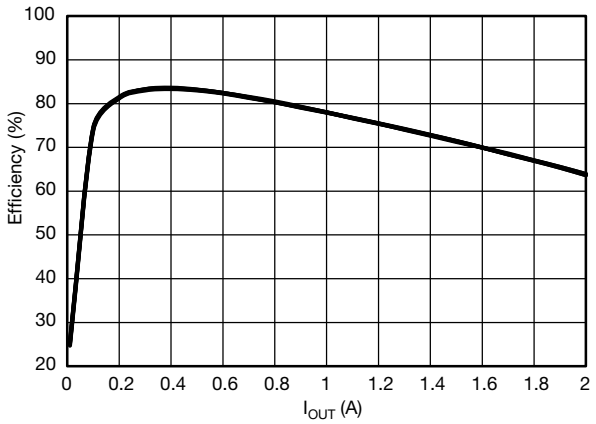


Fig. 14 - Efficiency vs. I_{OUT}
V_{IN} = 18 V, f_{SW} = 1 MHz

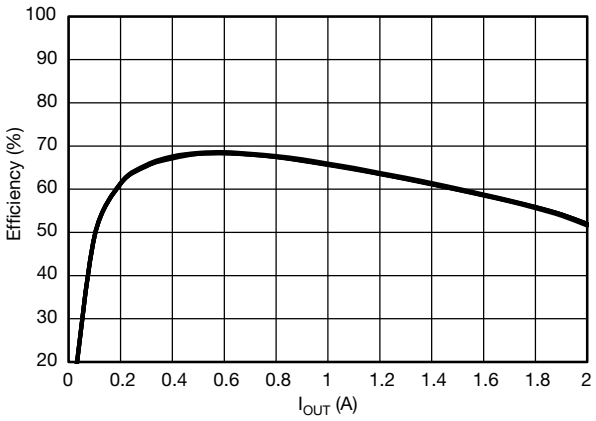


Fig. 15 - Efficiency vs. I_{OUT}
V_{IN} = 18 V, f_{SW} = 5 MHz

ELECTRICAL CHARACTERISTICS

(V_{IN} = 15 V, V_{OUT} = 2 V, V_{CIN} = V_{DRVx} = 5 V, I_{OUT} = 0.5 A, f_{SW} = 5 MHz, L = 4.7 µH, unless otherwise noted)

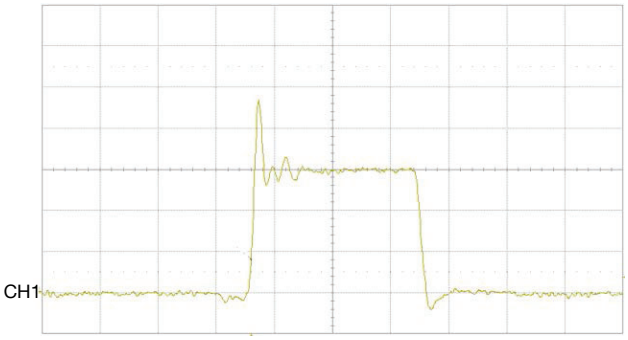


Fig. 16 - Output Switching Waveform
CH1 (YLLW) = SW1 (5 V/div.), Time = 10 ns/div.

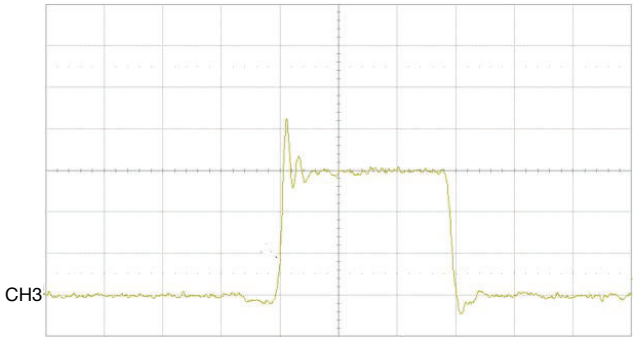


Fig. 19 - Output Switching Waveform
CH3 (YLLW) = SW3 (5 V/div.), Time = 10 ns/div.

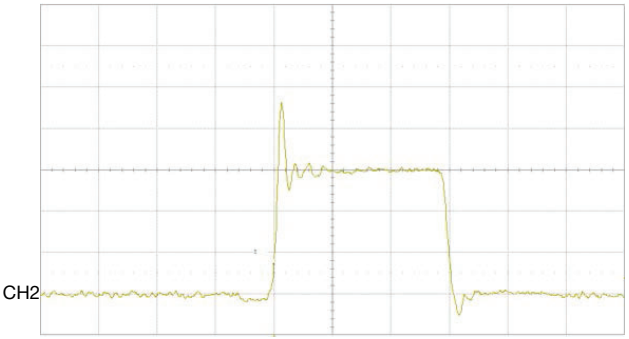


Fig. 17 - Output Switching Waveform
CH2 (YLLW) = SW2 (5 V/div.), Time = 10 ns/div.

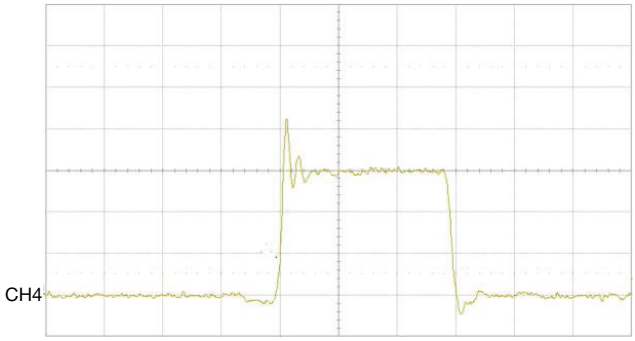


Fig. 20 - Output Switching Waveform
CH4 (YLLW) = SW4 (5 V/div.), Time = 10 ns/div.

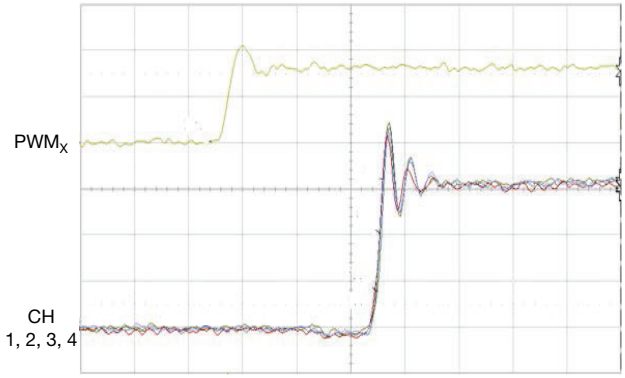


Fig. 18 - Propagation Delay - Rising (all channels)
CH1 = (VLT) = SW1 (5 V/div.), CH2 = (RED) = SW2 (5 V/div.), CH3 = (BLU) = SW3 (5 V/div.), CH4 = (GRN) = SW4 (5 V/div.), PWM_X (YLLW) = 2 V/div., Time = 5 ns/div.

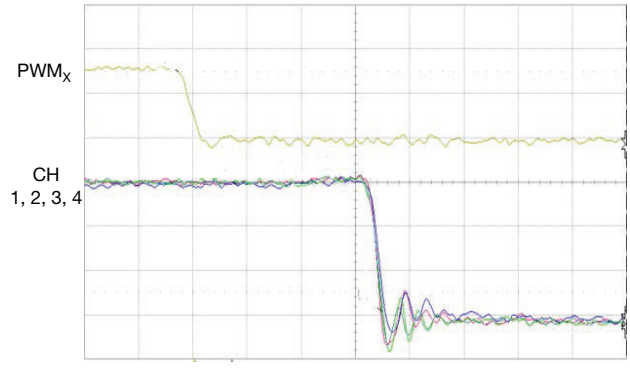


Fig. 21 - Propagation Delay - Falling (all channels)
CH1 = (VLT) = SW1 (5 V/div.), CH2 = (RED) = SW2 (5 V/div.), CH3 = (BLU) = SW3 (5 V/div.), CH4 = (GRN) = SW4 (5 V/div.), PWM_X (YLLW) = 2 V/div., Time = 5 ns/div.

DEMO BOARD SCHEMATIC

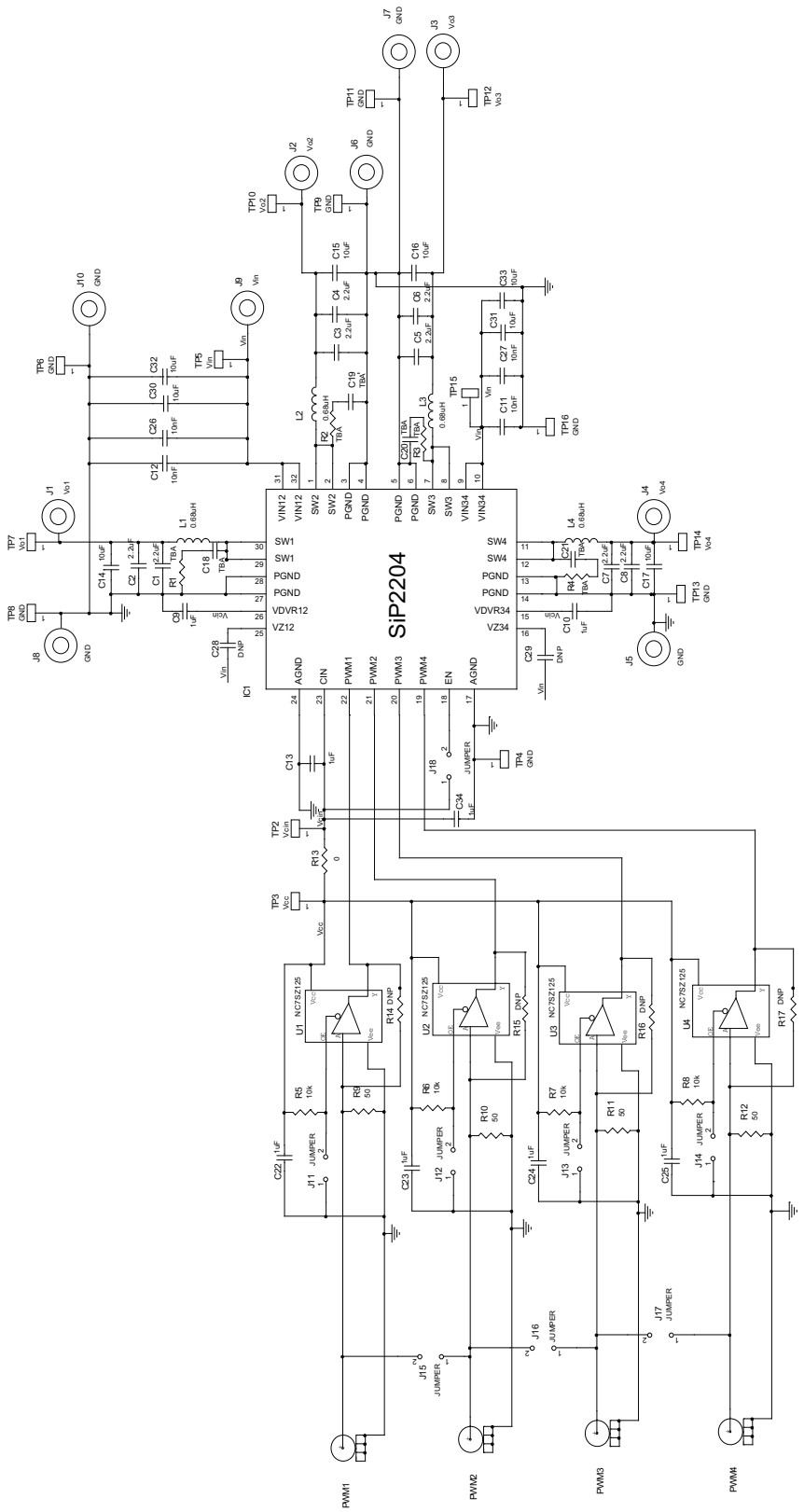


Fig. 22 - Reference Board Schematic for SiP2204

BILL OF MATERIALS

ITEM	QTY.	REFERENCE	COMPONENT VALUE	PCB FOOTPRINT
1	8	C1, C2, C3, C4, C5, C6, C7, C8	2.2 µF, 6.3 V	0805
2	4	C9, C10, C13, C34	1 µF, 6.3 V	0402
3	4	C11, C12, C26, C27	10 nF, 25 V	0805
4	4	C14, C15, C16, C17	10 µF, 6.3 V	1206
5	4	C18, C19, C20, C21	DNP	0603
6	4	C22, C23, C24, C25	1 µF, 10 V	0603
7	2	C28, C29	DNP	0603
8	4	C30, C31, C32, C33	10 µF, 25 V	1210
9	1	IC1	SiP2204	QFN5x5-32
10	1	J1	V_O1	Banana
11	1	J2	V_O2	Banana
12	1	J3	V_O3	Banana
13	1	J4	V_O4	Banana
14	5	J5, J6, J7, J8, J10	GND	Banana
15	1	J9	V_{IN}	Banana
16	8	J11, J12, J13, J14, J15, J16, J17, J18	JUMPER	Jumper2
17	4	L1, L2, L3, L4	4.7 µH	IHLP2525A
18	4	PWM1, PWM2, PWM3, PWM4	SMA connect	SMA
19	4	R1, R2, R3, R4	DNP	R0805-Vishay
20	4	R5, R6, R7, R8	10 kΩ	R0805-Vishay
21	4	R9, R10, R11, R12	50 Ω	R1206-Vishay
22	1	R13	0 Ω	R0805-Vishay
23	4	R14, R15, R16, R17	DNP	R0603-Vishay
24	1	TP2	V_{CIN}	TP30
25	1	TP3	V_{CC}	TP30
26	7	TP4, TP6, TP8, TP9, TP11, TP13, TP16	GND	TP30
27	2	TP5, TP15	V_{IN}	TP30
28	1	TP7	V_O1	TP30
29	1	TP10	V_O2	TP30
30	1	TP12	V_O3	TP30
31	1	TP14	V_O4	TP30
32	4	U1, U2, U3, U4	NC7SZ125	SOT23-5

PCB LAYOUT OF REFERENCE BOARD

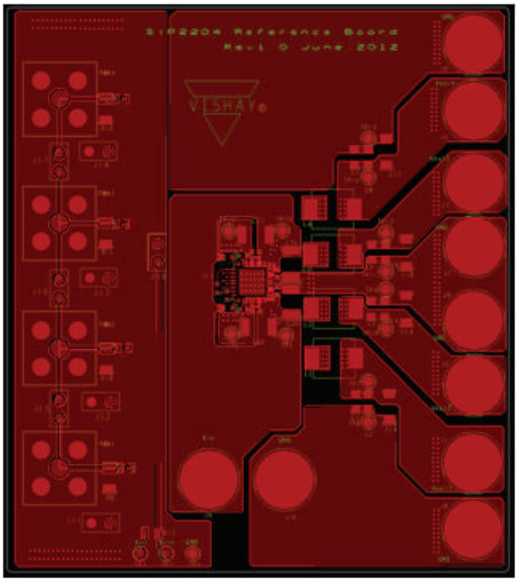


Fig. 23 - Top Layer

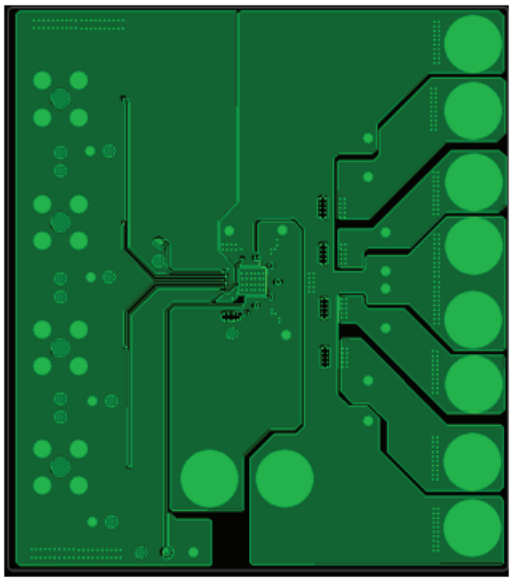


Fig. 25 - Inner 2

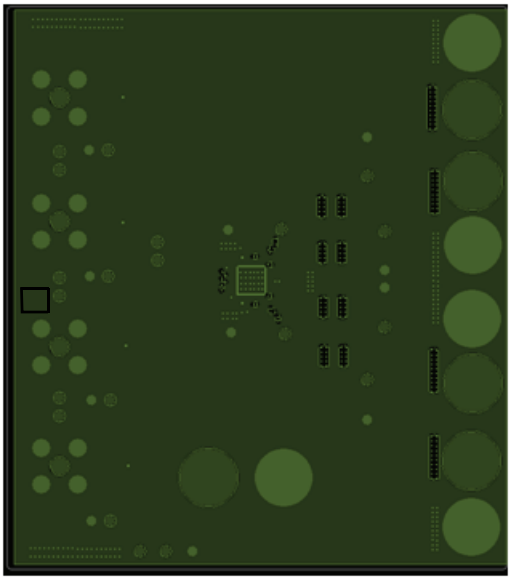


Fig. 24 - Inner 1

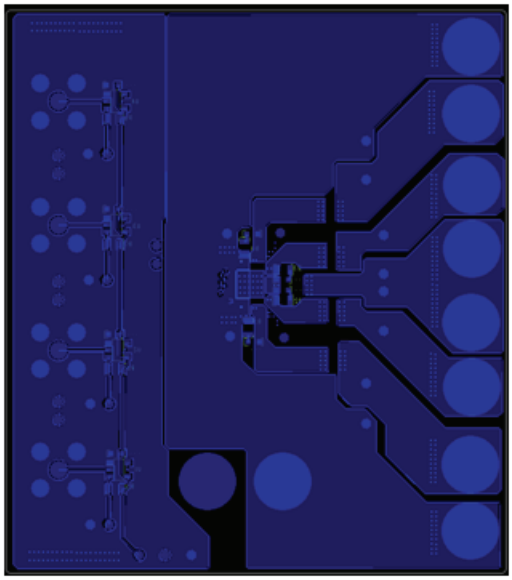


Fig. 26 - Bottom

PRODUCT SUMMARY	
Part number	SiP2204
Description	0.5 A power stage, 10 V_{IN} to 24 V_{IN}, 3.3 V and 5.5 V PWM with - mode
Input voltage min. (V)	10
Input voltage max. (V)	24
Continuous current rating max. (A)	0.5
Switch frequency max. (kHz)	5000
Enable (yes / no)	YES
Monitoring features	-
Protection	UVLO
Light load mode	-
Pulse-width modulation (V)	3.3 and 5
Package type	QFN32-55
Package size (W, L, H) (mm)	5.0 x 5.0 x 0.85
Status code	2
Product type	VRPower (DrMOS)
Applications	Computer, industrial, networking

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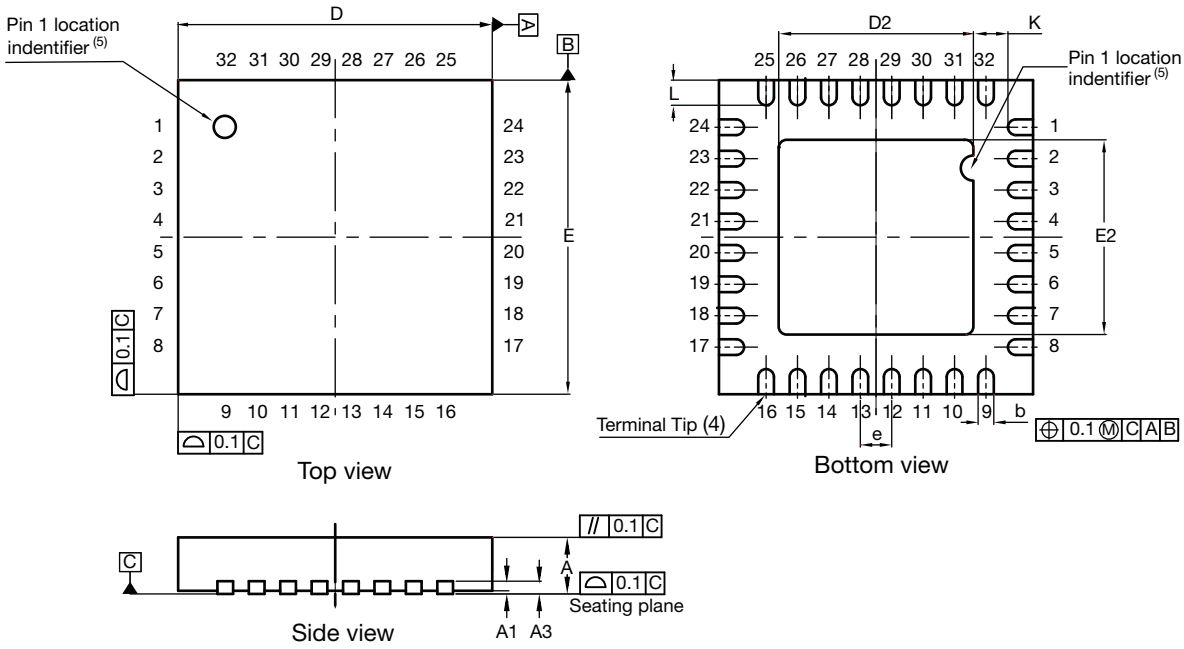
QFN32 5 x 5 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
D2	3.00	3.10	3.20	0.118	0.122	0.126
e	0.50 BSC			0.020 BSC		
E	5.00 BSC			0.197 BSC		
E2	3.00	3.10	3.20	0.118	0.122	0.126
K	0.20	-	-	0.008	-	-
L	0.30	0.40	0.50	0.012	0.016	0.020
N (3)	32			32		
Nd (3)	8			8		
Ne (3)	8			8		

Notes

(1) Use millimeters as the primary measurement
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994
(3) N is the number of terminals,
Nd is the number of terminals in X-direction and
Ne is the number of terminals in Y-direction.
(4) Dimension b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip
(5) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
(6) Package warpage max. 0.05 mm

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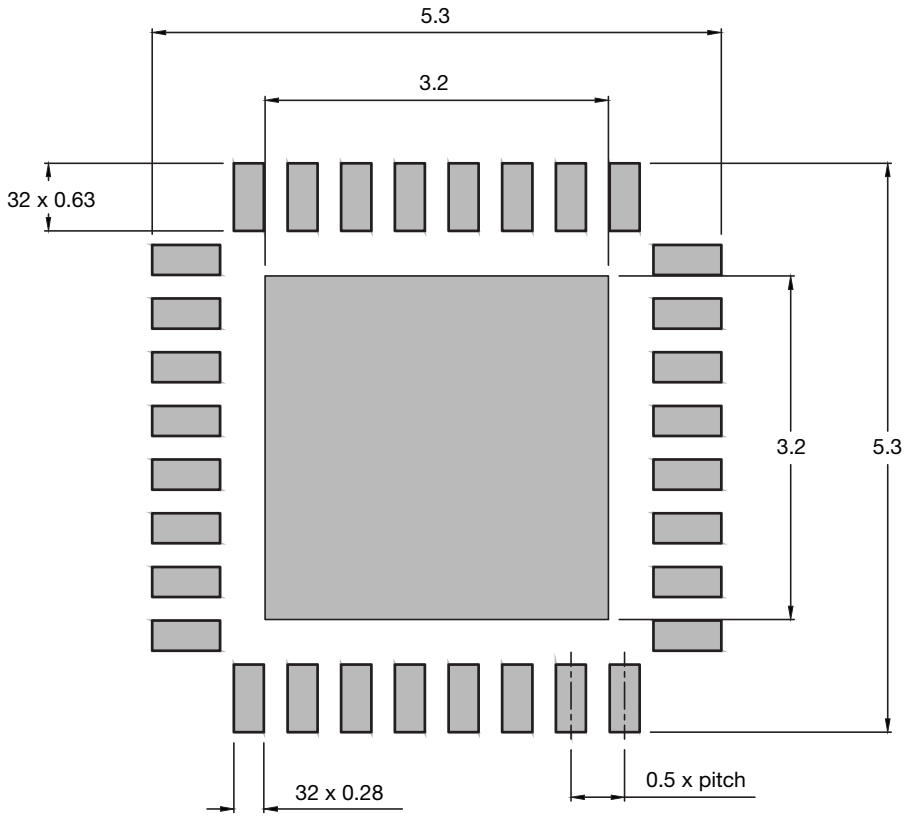
DWG: 6027

Recommended Land Pattern QFN32 5 x 5



Dimensions are in millimeters

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