P-Channel 20 V (D-S) MOSFET

DESCRIPTION
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55°C to 125°C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55°C to +125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC

Note
- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.
### SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

<table>
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<th>PARAMETER</th>
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<th>SIMULATED DATA</th>
<th>MEASURED DATA</th>
<th>UNIT</th>
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<tr>
<td><strong>Static</strong></td>
<td></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>Gate Threshold Voltage</td>
<td>V_GS(th)</td>
<td>V_DS = V_GS, I_D = - 250 μA</td>
<td>0.70</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Drain-Source On-State Resistance</td>
<td>R_DS(on)</td>
<td>V_GS = - 4.5 V, I_D = - 3.2 A</td>
<td>0.052</td>
<td>0.050</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_GS = - 2.5 V, I_D = - 2.8 A</td>
<td>0.067</td>
<td>0.065</td>
<td></td>
</tr>
<tr>
<td>Forward Transconductance a</td>
<td>g_fs</td>
<td>V_DS = - 10 V, I_D = - 3.2 A</td>
<td>11</td>
<td>12</td>
<td>S</td>
</tr>
<tr>
<td>Diode Forward Voltage</td>
<td>V_SD</td>
<td>I_S = - 3 A</td>
<td>- 0.80</td>
<td>- 0.80</td>
<td>V</td>
</tr>
<tr>
<td><strong>Dynamic b</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Gate Charge</td>
<td>Q_g</td>
<td>V_DS = - 10 V, V_GS = - 8 V, I_D = - 5.3 A</td>
<td>9</td>
<td>14</td>
<td>nC</td>
</tr>
<tr>
<td>Gate-Source Charge</td>
<td>Q_gs</td>
<td>V_DS = - 10 V, V_GS = - 4.5 V, I_D = - 5.3 A</td>
<td>0.8</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>Gate-Drain Charge</td>
<td>Q_gd</td>
<td></td>
<td>3.1</td>
<td>3.1</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

Note
- Dots and squares represent measured data.
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