

N- and P-Channel 30 V (D-S) 175 °C MOSFET

DESCRIPTION

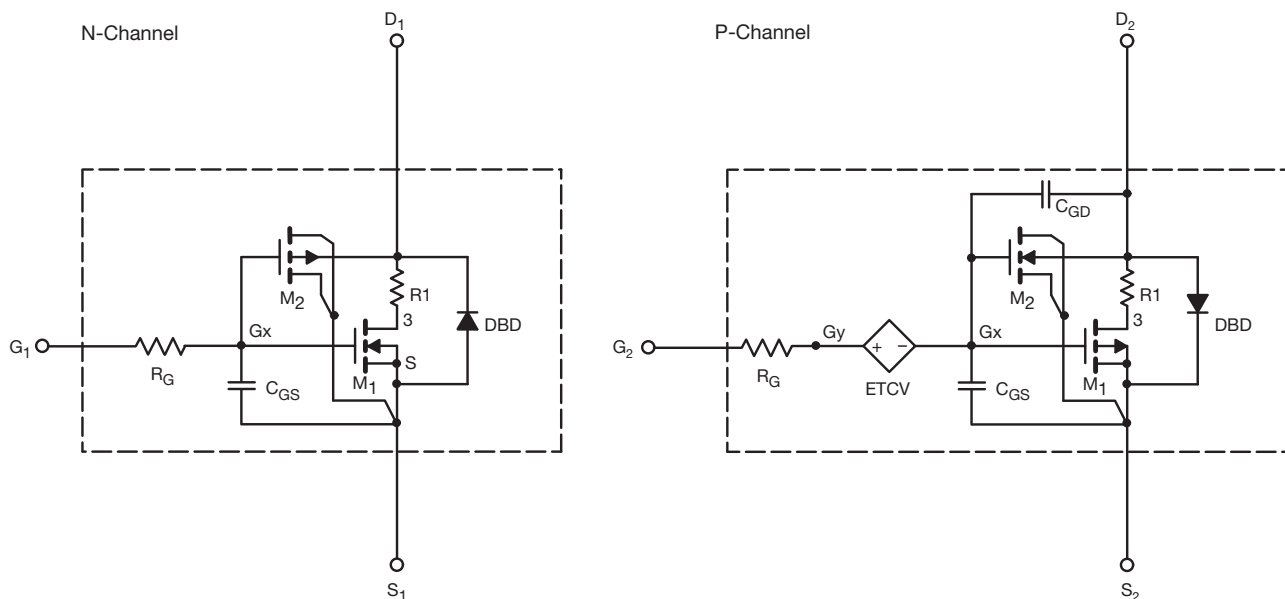
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	2.2	-	V
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	2.4	-	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 4.9 A	N-Ch	0.048	0.046	Ω
		V _{GS} = - 10 V, I _D = - 3.5 A	P-Ch	0.056	0.056	
		V _{GS} = 4.5 V, I _D = 4.1 A	N-Ch	0.084	0.083	
		V _{GS} = - 4.5 V, I _D = - 2.5 A	P-Ch	0.154	0.157	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 4.9 A	N-Ch	9	9.8	S
		V _{DS} = - 15 V, I _D = - 3.5 A	P-Ch	7	5.5	
Diode Forward Voltage ^a	V _{SD}	I _S = 2 A, V _{GS} = 0 V	N-Ch	0.80	0.80	V
		I _S = - 1.5 A, V _{GS} = 0 V	P-Ch	- 0.81	- 0.80	
Dynamic ^b						
Input Capacitance	C _{iss}	N-Channel V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	452	444	pF
Output Capacitance	C _{oss}		P-Ch	385	384	
		Reverse Transfer Capacitance	C _{rss}	P-Channel V _{DS} = - 25 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	
P-Ch	96				100	
Total Gate Charge	Q _g	N-Channel V _{DS} = 15 V, V _{GS} = 10 V, I _D = 3.9 A	N-Ch	7	8.7	nC
			P-Ch	8	9.7	
Gate-Source Charge	Q _{gs}	P-Channel V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 2.5 A	N-Ch	1.9	1.9	
			P-Ch	1.8	1.8	
Gate-Drain Charge	Q _{gd}		N-Ch	1.6	1.6	
			P-Ch	2.3	2.3	

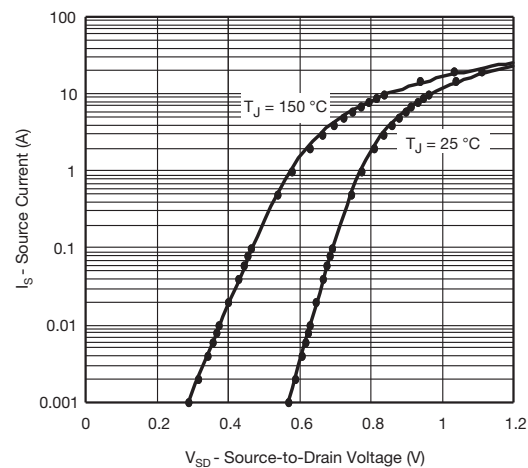
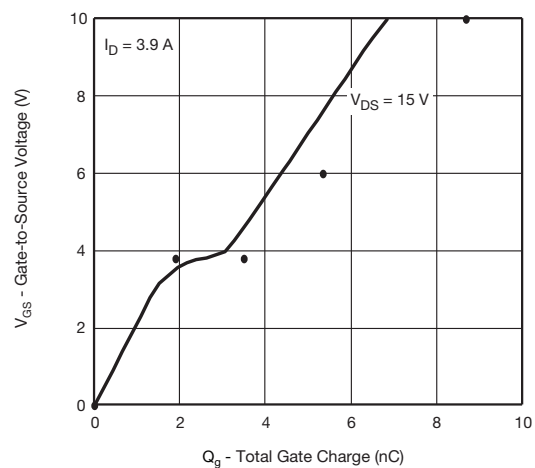
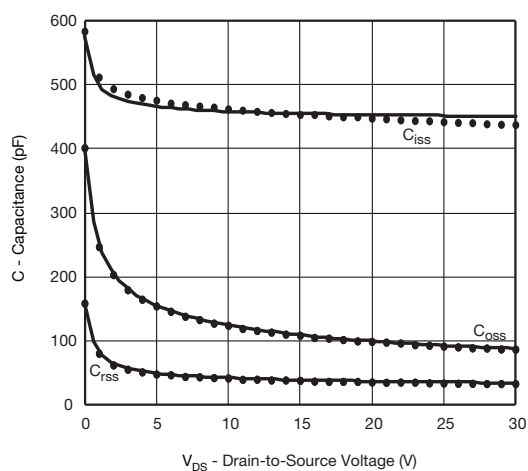
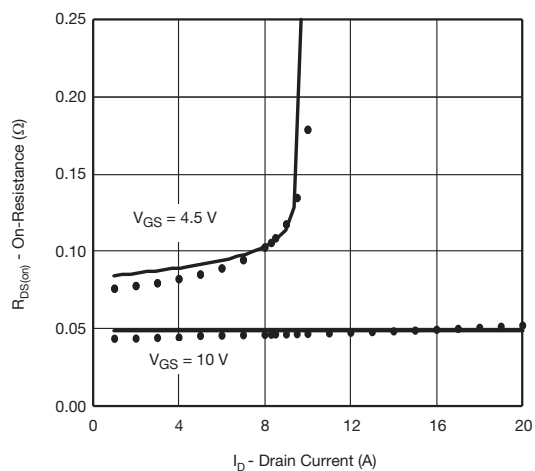
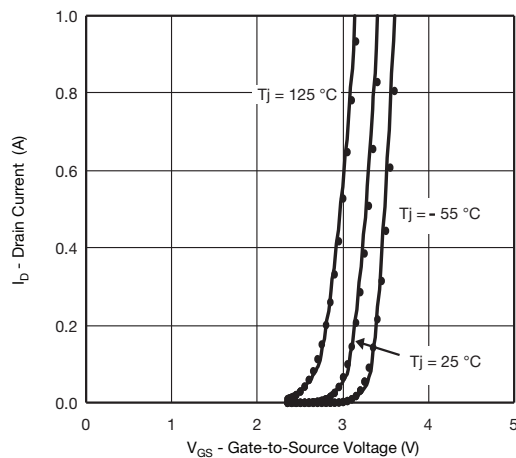
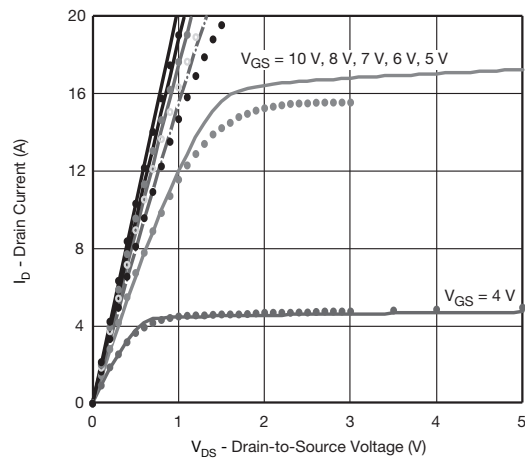
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25^\circ\text{C}$, unless otherwise noted)

N-Channel MOSFET



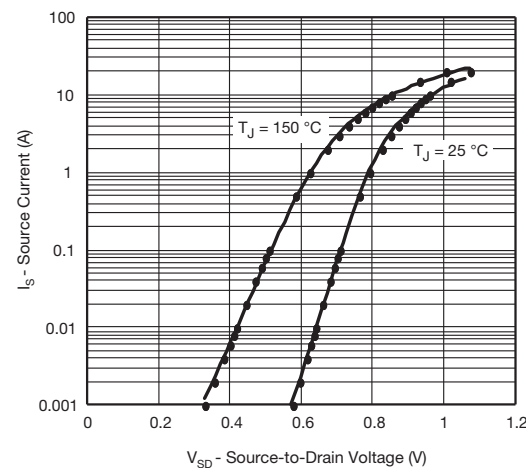
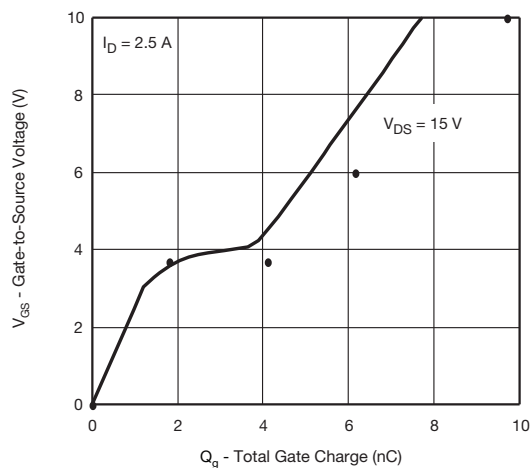
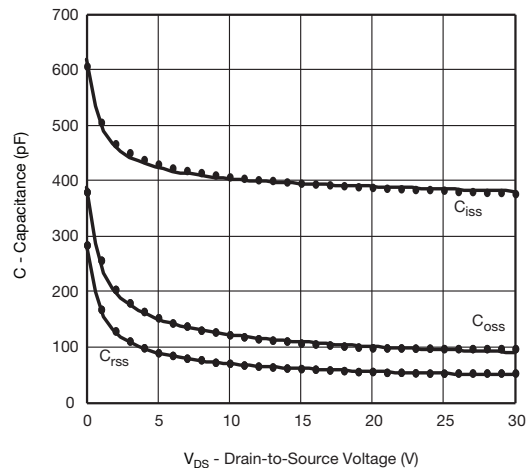
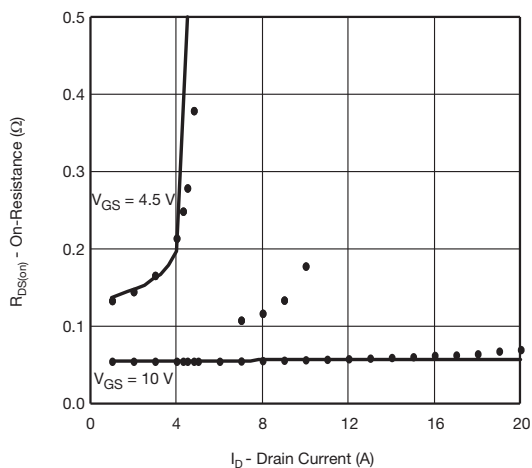
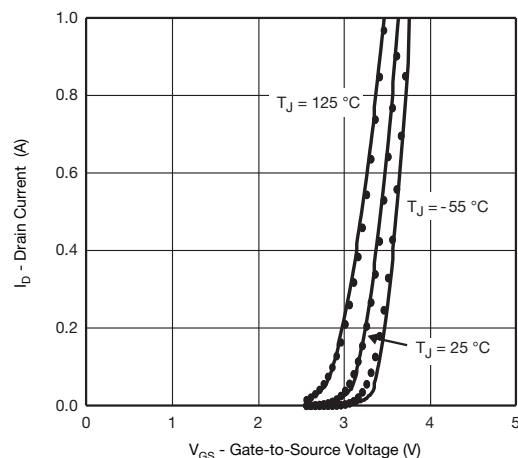
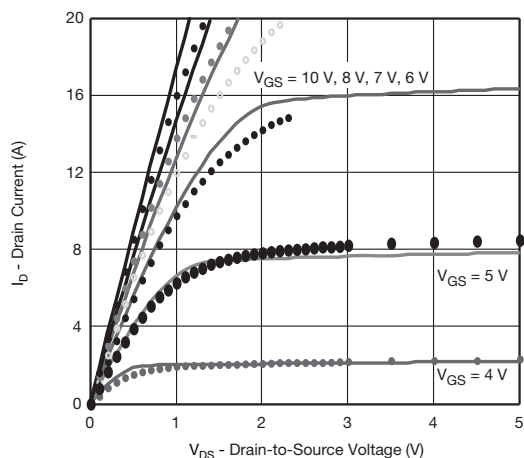
Note

- Dots and squares represent measured data.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25^\circ\text{C}$, unless otherwise noted)

P-Channel MOSFET



Note

- Dots and squares represent measured data.