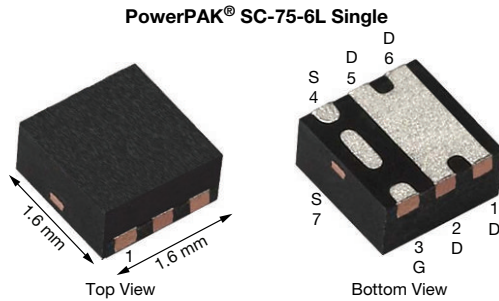


P-Channel 12 V (D-S) MOSFET



Marking code: BO

PRODUCT SUMMARY	
V_{DS} (V)	-12
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.0255
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -3.7$ V	0.0280
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -2.5$ V	0.0360
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.8$ V	0.0600
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.5$ V	0.1150
Q_g typ. (nC)	13.4
I_D (A) ^a	9
Configuration	Single

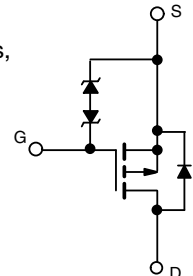
FEATURES

- TrenchFET® power MOSFET
- Thermally enhanced PowerPAK® SC-75 package
 - Small footprint area
 - Low on-resistance
- Typical ESD performance 2500 V
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Portable devices such as smart phones, tablet PCs, and mobile computing
 - Battery switch
 - Load switch
 - Power management



P-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SC-75
Lead (Pb)-free and halogen-free	SiB441EDK-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-12	V
Gate-source voltage	V_{GS}	± 8	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	-9 ^a
		$T_C = 70$ °C	-9 ^a
		$T_A = 25$ °C	-8.3 ^{b, c}
		$T_A = 70$ °C	-6.6 ^{b, c}
Pulsed drain current ($t = 300$ μ s)	I_{DM}	-40	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	-2 ^{b, c}
Maximum power dissipation	P_D	$T_C = 25$ °C	13
		$T_C = 70$ °C	8.4
		$T_A = 25$ °C	2.4 ^{b, c}
		$T_A = 70$ °C	1.6 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	$t \leq 5$ s	R_{thJA}	41	51	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	7.5	9.5	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 5$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 105 °C/W



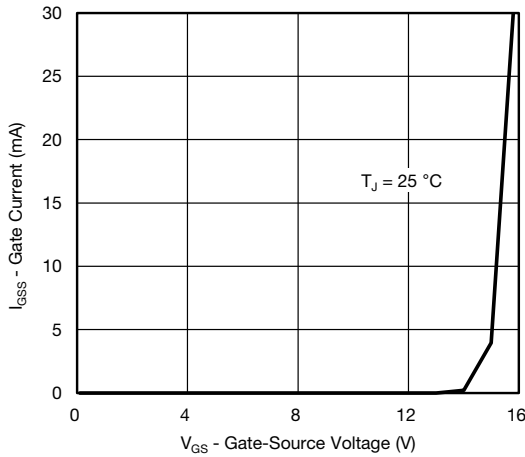
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-12	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$	-	-5	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	2.7	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4	-	-0.9	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	-	-	± 4	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$	-	-	± 1	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	-10	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-15	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$	-	0.0210	0.0255	Ω
		$V_{GS} = -3.7\text{ V}, I_D = -4\text{ A}$	-	0.0230	0.0280	
		$V_{GS} = -2.5\text{ V}, I_D = -2\text{ A}$	-	0.0290	0.0360	
		$V_{GS} = -1.8\text{ V}, I_D = -2\text{ A}$	-	0.0420	0.0600	
		$V_{GS} = -1.5\text{ V}, I_D = -0.5\text{ A}$	-	0.0570	0.1150	
Forward transconductance ^a	g_{fs}	$V_{DS} = -6\text{ V}, I_D = -4\text{ A}$	-	17	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = -6\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1180	-	pF
Output capacitance	C_{oss}		-	265	-	
Reverse transfer capacitance	C_{rss}		-	250	-	
Total gate charge	Q_g	$V_{DS} = -6\text{ V}, V_{GS} = -8\text{ V}, I_D = -2.1\text{ A}$	-	22.1	33	nC
		$V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -2.1\text{ A}$	-	13.4	20	
Gate-source charge	Q_{gs}		-	1.6	-	
Gate-drain charge	Q_{gd}		-	3.4	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	2.2	11	22	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 2.7\text{ }\Omega$ $I_D \cong -2.2\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$	-	22	45	ns
Rise time	t_r		-	42	85	
Turn-off delay time	$t_{d(off)}$		-	60	120	
Fall time	t_f		-	50	100	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 2.7\text{ }\Omega$ $I_D \cong -2.2\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$	-	7	15	
Rise time	t_r		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	60	120	
Fall time	t_f		-	52	100	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	-9	A
Pulse diode forward current	I_{SM}		-	-	-40	
Body diode voltage	V_{SD}	$I_S = -2.2\text{ A}, V_{GS} = 0\text{ V}$	-	-0.85	-1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = -2.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	30	60	ns
Body diode reverse recovery charge	Q_{rr}		-	12	25	nC
Reverse recovery fall time	t_a		-	9	-	ns
Reverse recovery rise time	t_b		-	11	-	

Notes

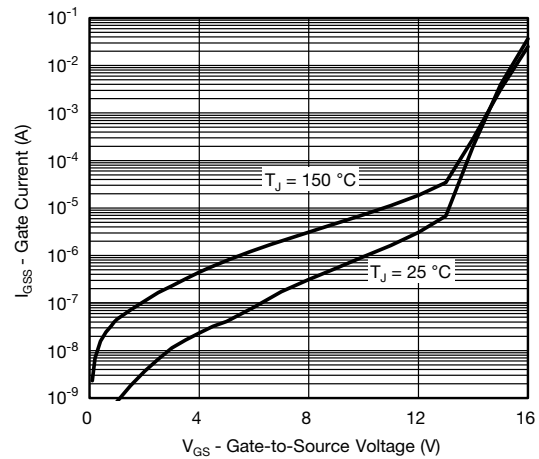
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

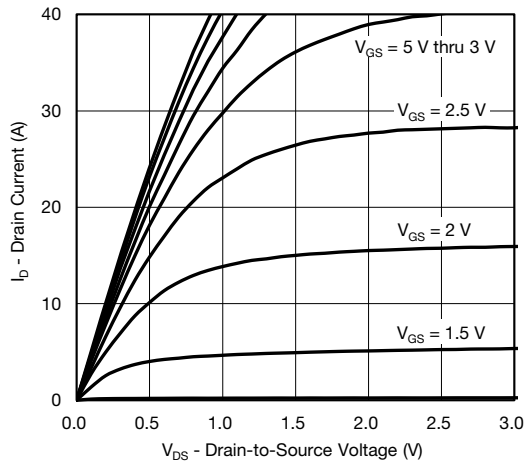
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



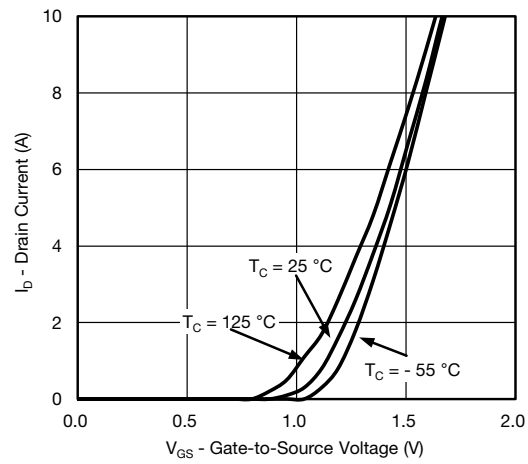
Gate Current vs. Gate-Source Voltage



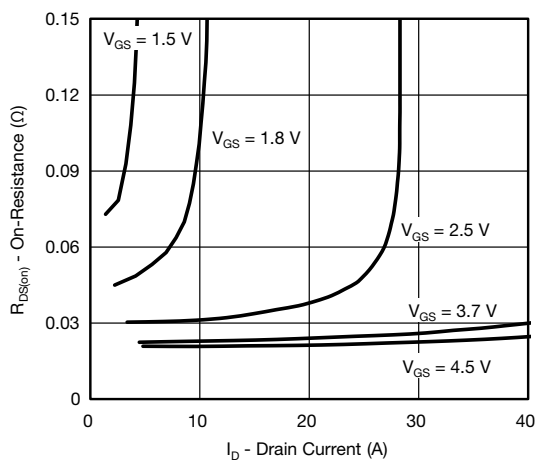
Gate Current vs. Gate-Source Voltage



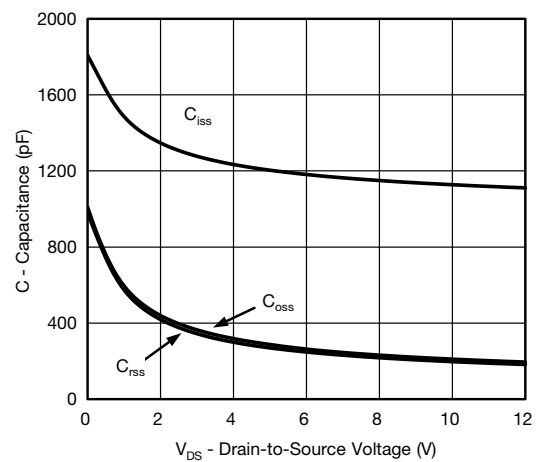
Output Characteristics



Transfer Characteristics



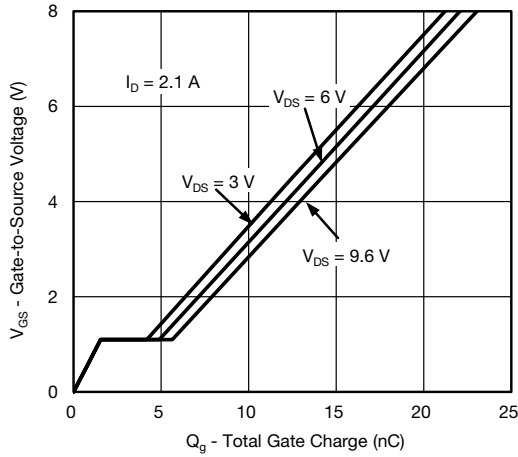
On-Resistance vs. Drain Current



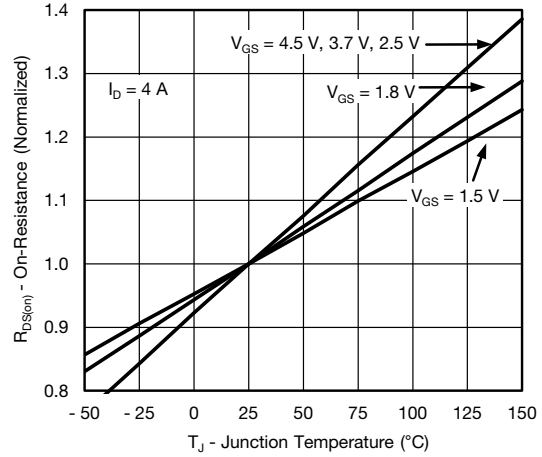
Capacitance



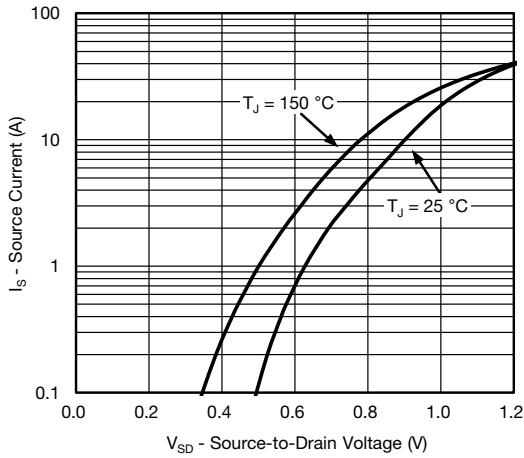
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



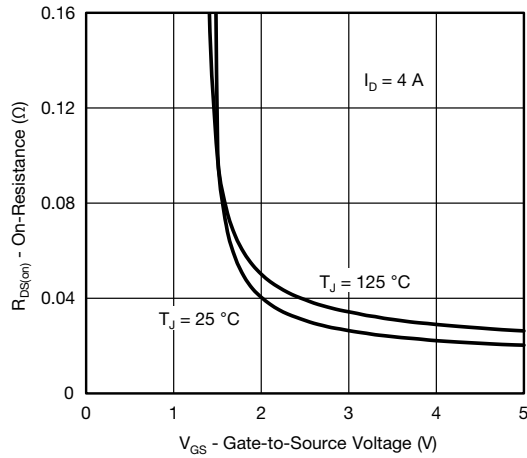
Gate Charge



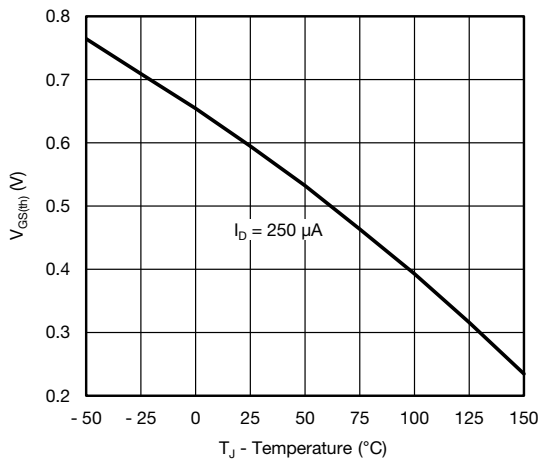
On-Resistance vs. Junction Temperature



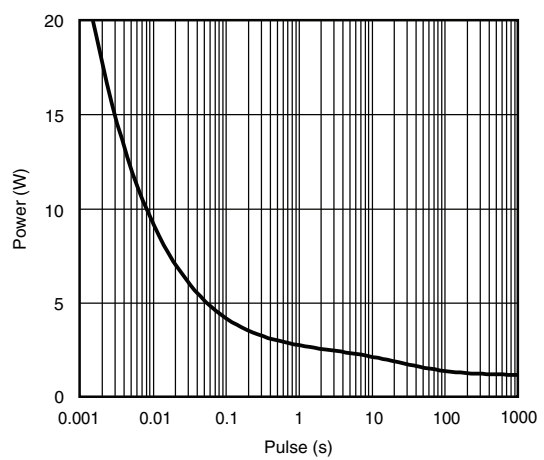
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

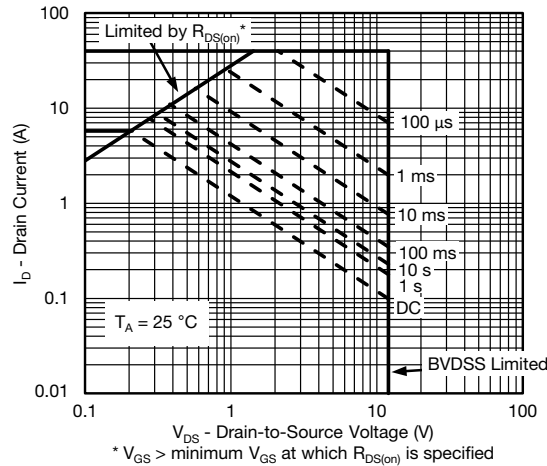


Threshold Voltage

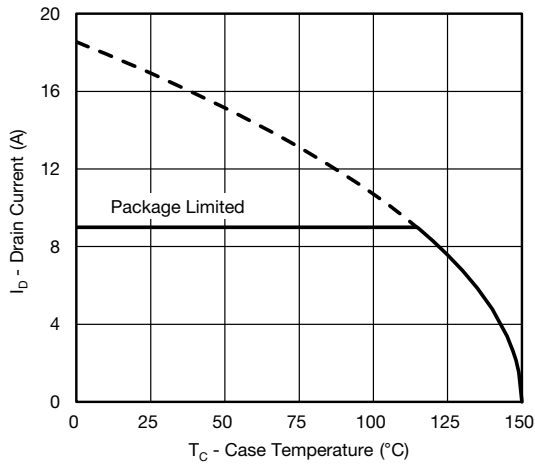


Single Pulse Power, Junction-to-Ambient

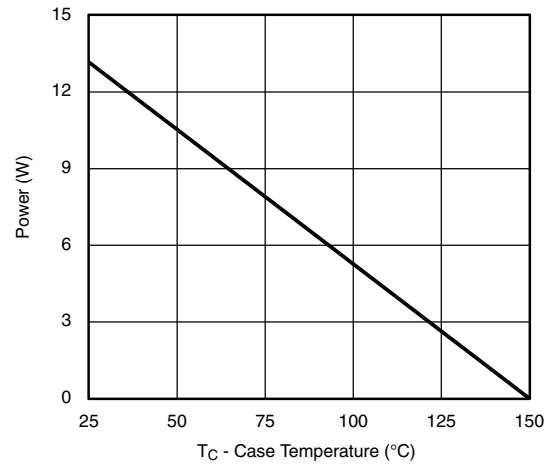
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating ^a



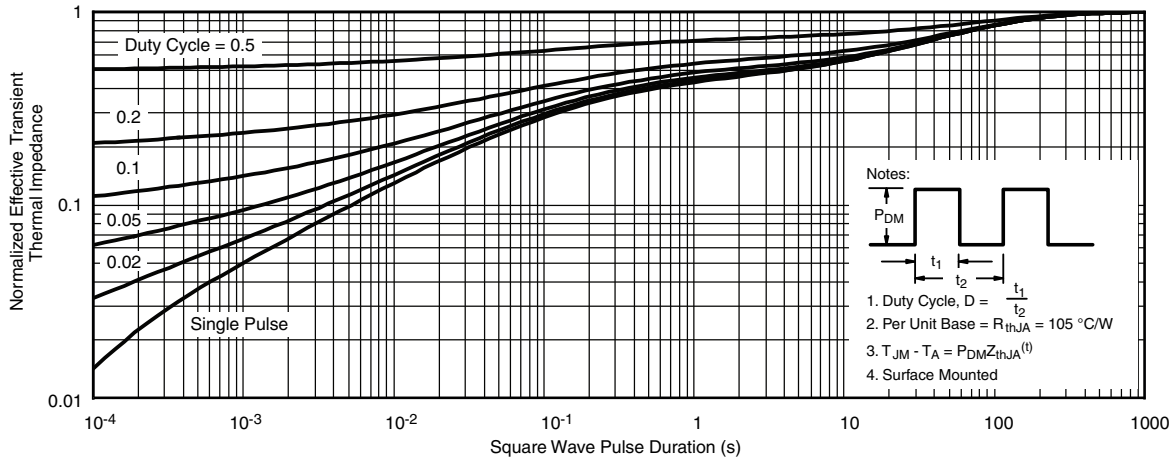
Power Derating

Note

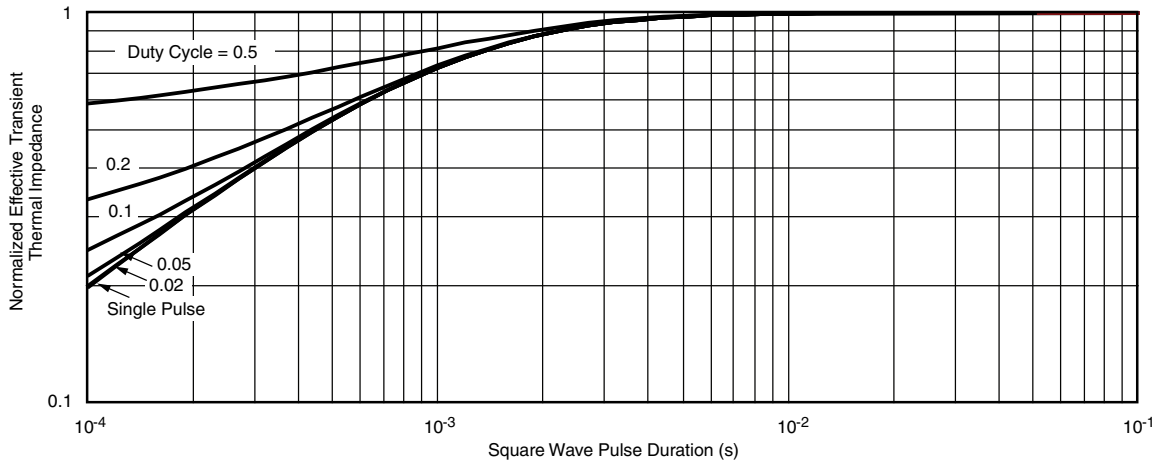
- a. The power dissipation P_D is based on $T_J \text{ max.} = 150 \text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62821.



PowerPAK® SC75-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- Notes:
 1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 – Rev. C, 06-Aug-07
 DWG: 5935

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Single



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