

N- and P-Channel 40 V (D-S) MOSFET

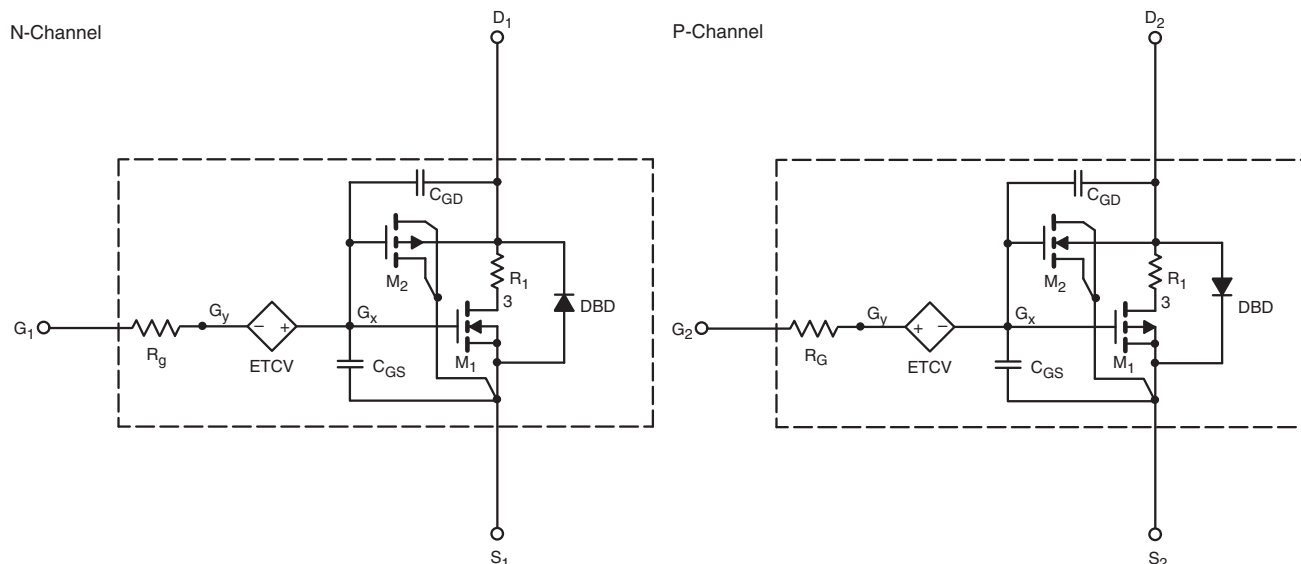
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.1	-	V
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	1.6	-	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 6.8 A	N-Ch	0.020	0.020	Ω
		V _{GS} = - 10 V, I _D = - 8 A	P-Ch	0.021	0.021	
		V _{GS} = 4.5 V, I _D = 6.6 A	N-Ch	0.022	0.022	
		V _{GS} = - 4.5 V, I _D = - 5 A	P-Ch	0.027	0.027	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 6.8 A	N-Ch	22	27	S
		V _{DS} = - 15 V, I _D = - 6.7 A	P-Ch	22	25	
Diode Forward Voltage ^a	V _{SD}	I _S = 5.4 A, V _{GS} = 0 V	N-Ch	0.80	0.81	V
		I _S = - 2 A, V _{GS} = 0 V	P-Ch	- 0.77	- 0.77	
Dynamic ^b						
Input Capacitance	C _{iss}	N-Channel V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = - 20 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	695	690	pF
Output Capacitance	C _{oss}		P-Ch	2002	2000	
			N-Ch	117	115	
Reverse Transfer Capacitance	C _{rss}		P-Ch	240	240	
		N-Ch	42	41		
Total Gate Charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 10 A V _{DS} = - 20 V, V _{GS} = - 10 V, I _D = - 10 A N-Channel V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 10 A P-Channel V _{DS} = - 20 V, V _{GS} = - 4.5 V, I _D = - 10 A	P-Ch	201	202	nC
			N-Ch	12	13.3	
			P-Ch	41	41.5	
			N-Ch	6	6.5	
Gate-Source Charge	Q _{gs}	P-Ch	22	21.7		
		N-Ch	2.3	2.3		
Gate-Drain Charge	Q _{gd}	P-Ch	5.6	5.6		
		N-Ch	1.7	1.7		
		P-Ch	9.8	9.8		

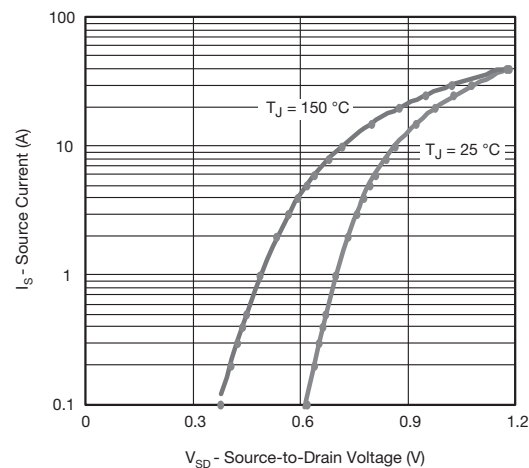
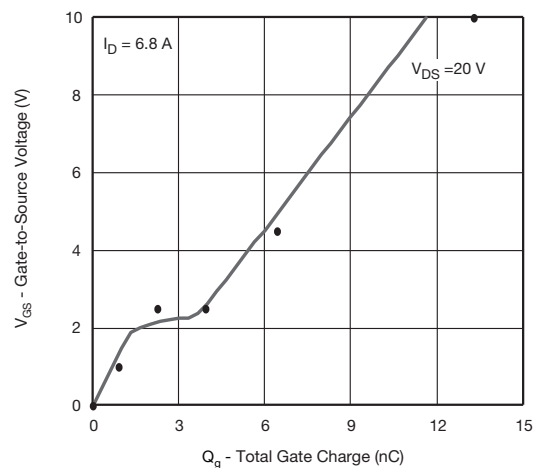
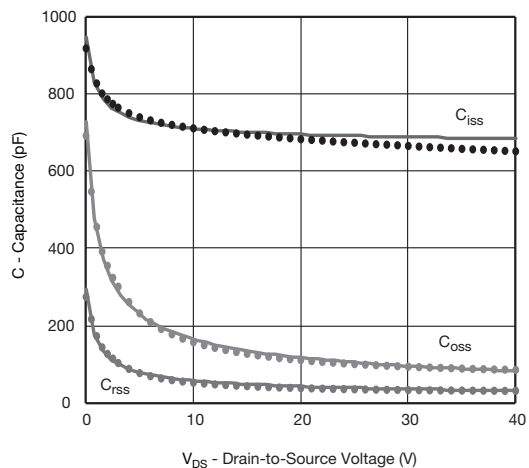
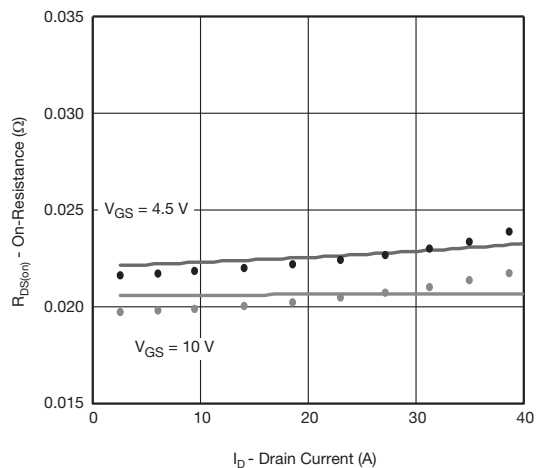
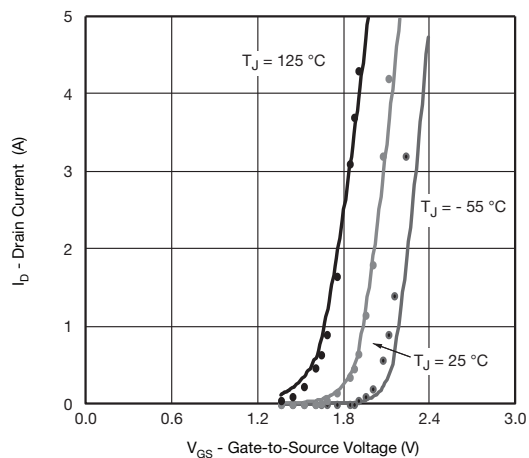
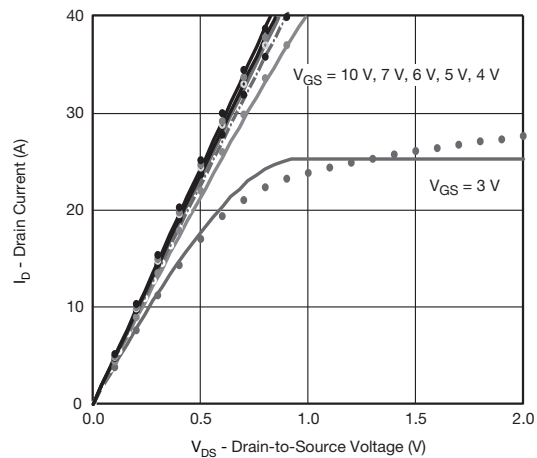
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ \%$.
b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25^\circ\text{C}$, unless otherwise noted

N-Channel MOSFET



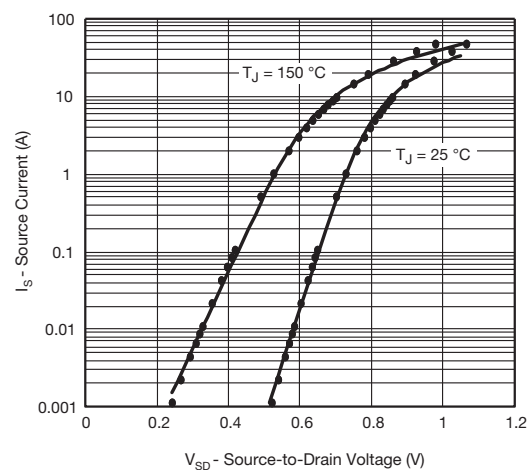
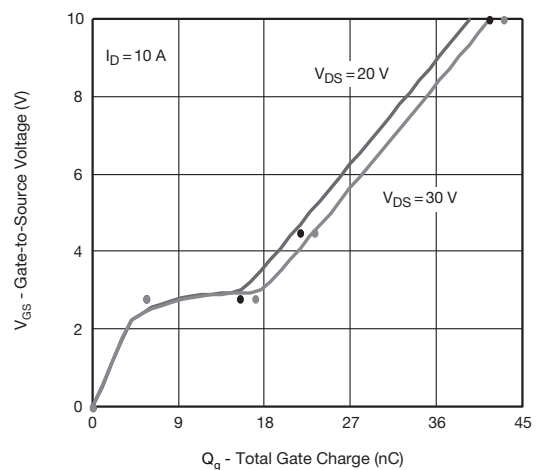
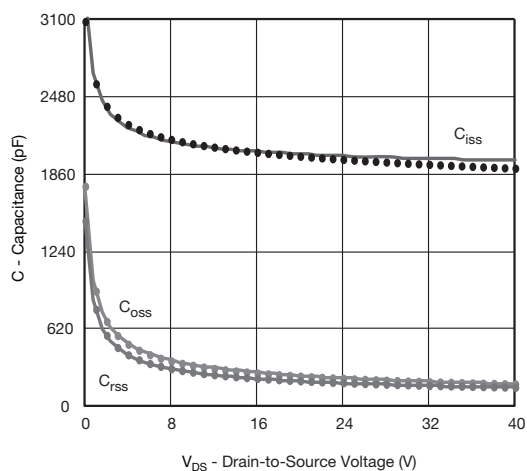
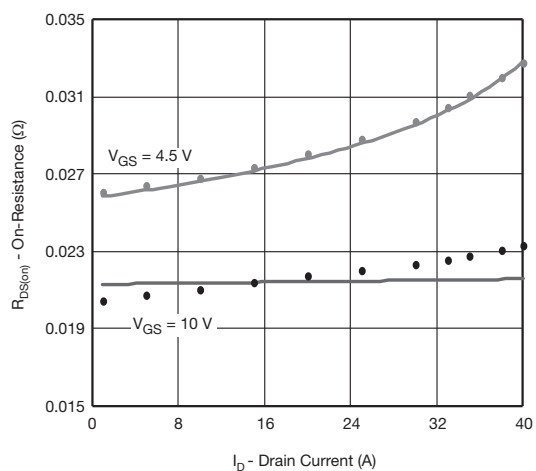
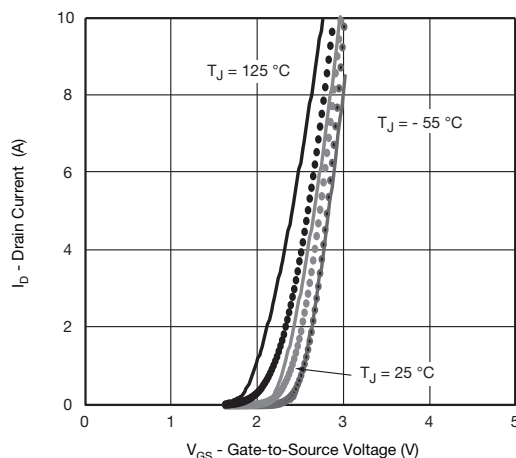
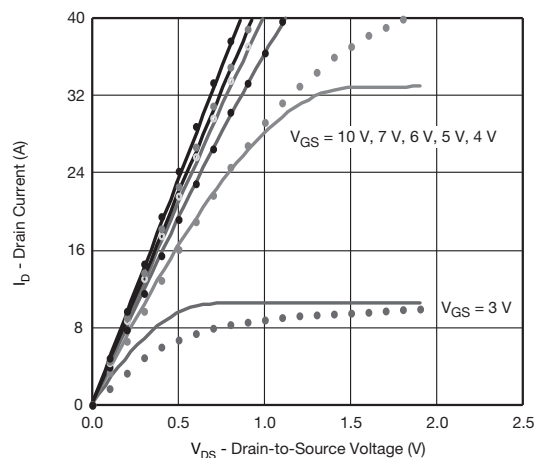
Note

- Dots and squares represent measured data.



COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25^\circ\text{C}$, unless otherwise noted

P-Channel MOSFET



Note

- Dots and squares represent measured data.