

Dual N-Channel 30 V (D-S) MOSFET

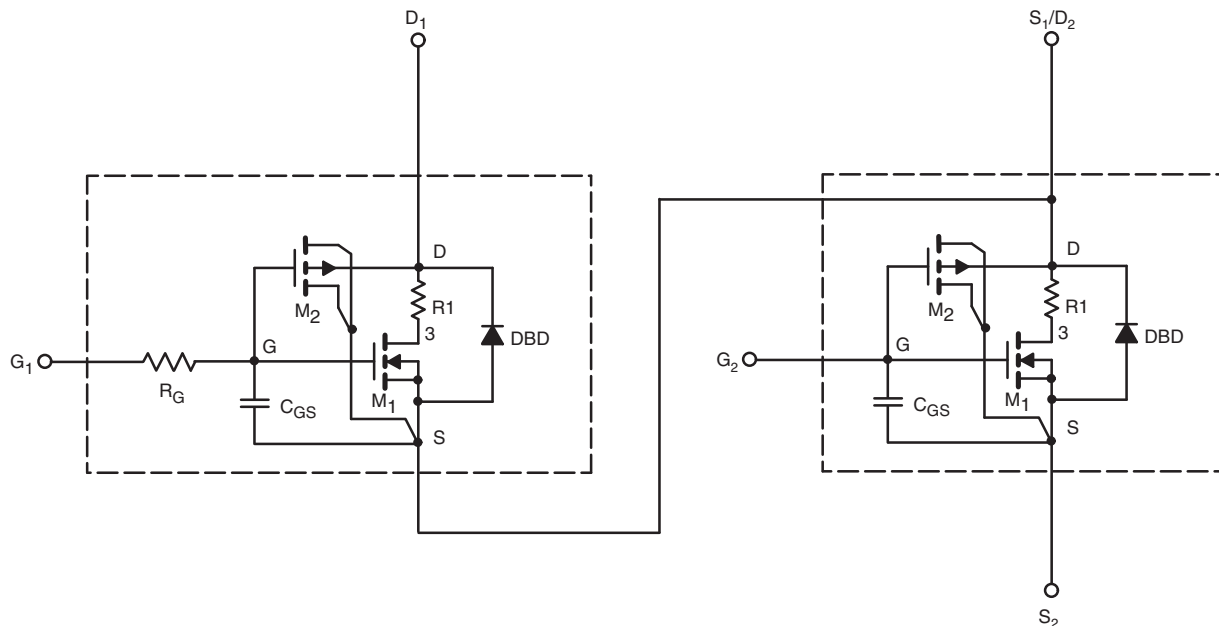
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1.5	-	V
			Ch-2	1.2	-	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	Ch-1	0.0078	0.0075	Ω
			Ch-2	0.0032	0.0032	
			Ch-1	0.0100	0.0105	
			Ch-2	0.0041	0.0043	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 15 A	Ch-1	42	48	S
			Ch-2	70	70	
Diode Forward Voltage ^b	V _{SD}	I _S = 10 A, V _{GS} = 0 V	Ch-1	0.79	0.80	V
			Ch-2	0.74	0.80	
Dynamic^b						
Input Capacitance	C _{iss}	Channel 1 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	827	830	pF
			Ch-2	2350	2370	
Output Capacitance	C _{oss}	Channel 2 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	190	185	
			Ch-2	482	475	
Reverse Transfer Capacitance	C _{rss}	Channel 1 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	81	80	
			Ch-2	219	220	
Total Gate Charge	Q _g	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 15 A	Ch-1	15	15.6	nC
			Ch-2	41	43	
		Channel 1 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 15 A	Ch-1	7.4	7.7	
			Ch-2	21	21.2	
Gate-Source Charge	Q _{gs}	Channel 2 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A	Ch-1	2.6	2.6	
			Ch-2	7	7	
Gate-Drain Charge	Q _{gd}	Channel 1 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A	Ch-1	3	3	
			Ch-2	7.4	7.4	

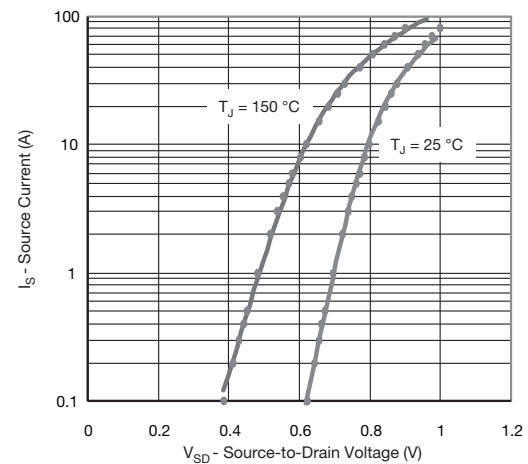
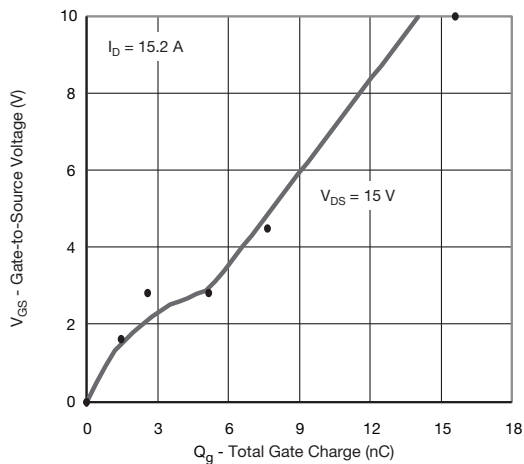
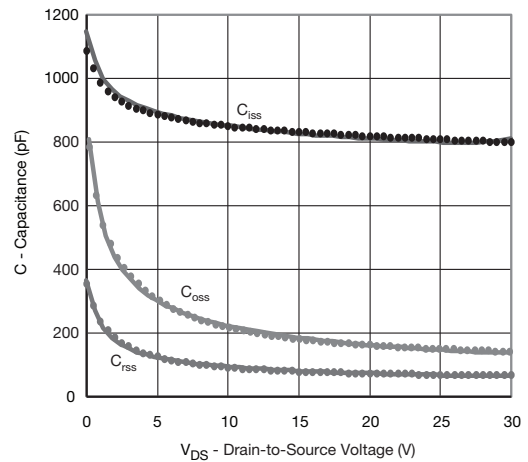
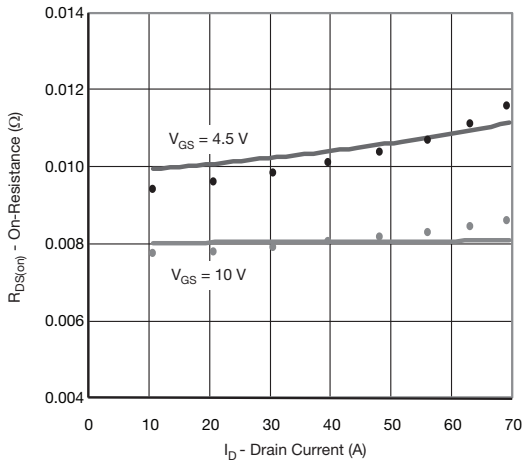
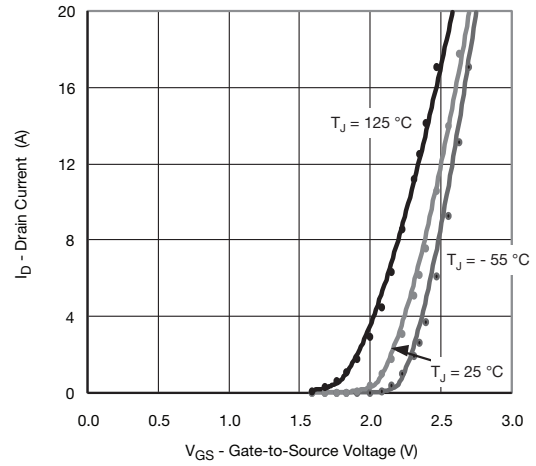
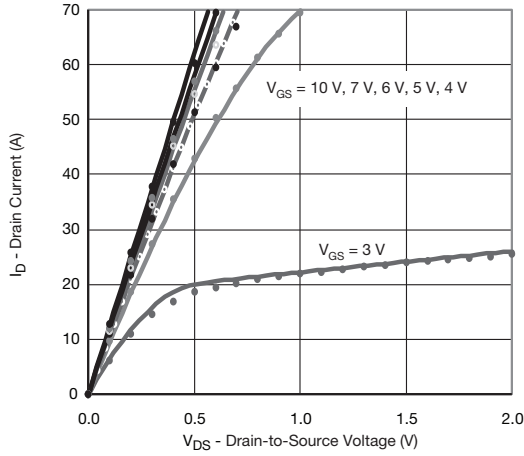
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Channel 1



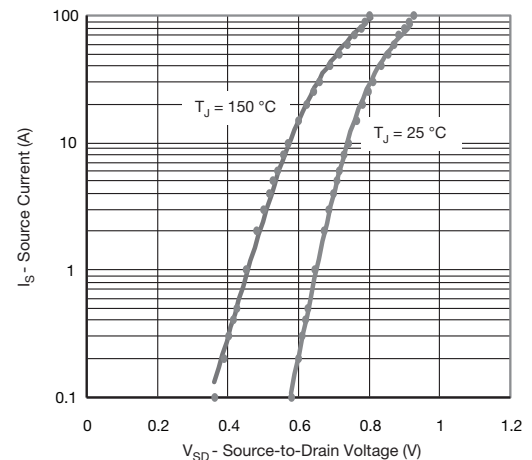
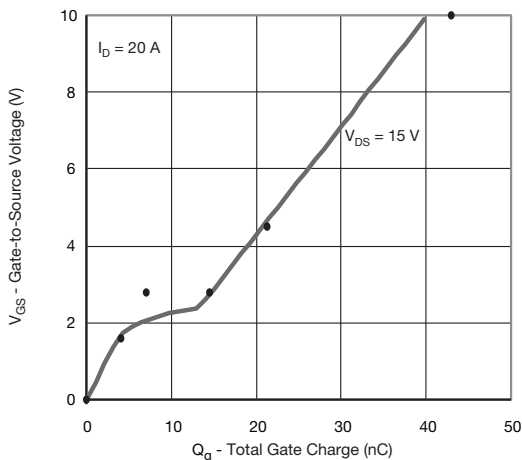
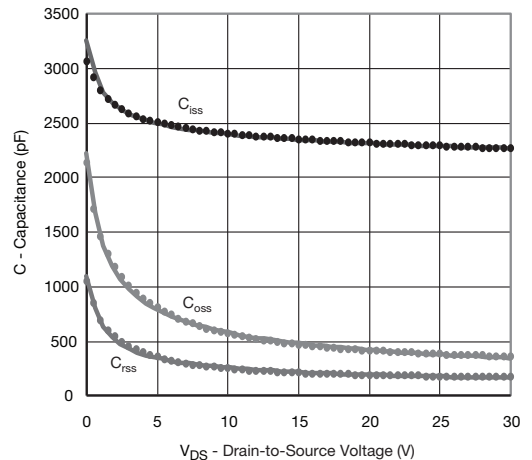
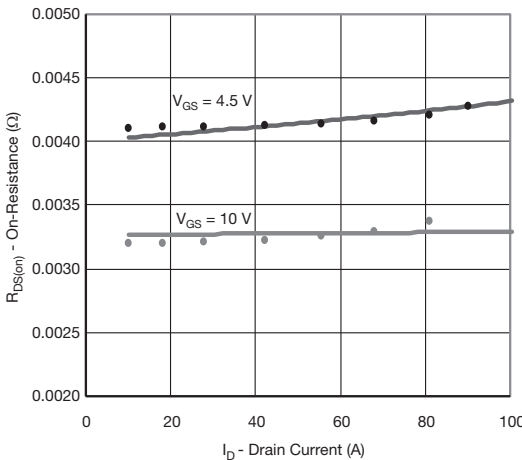
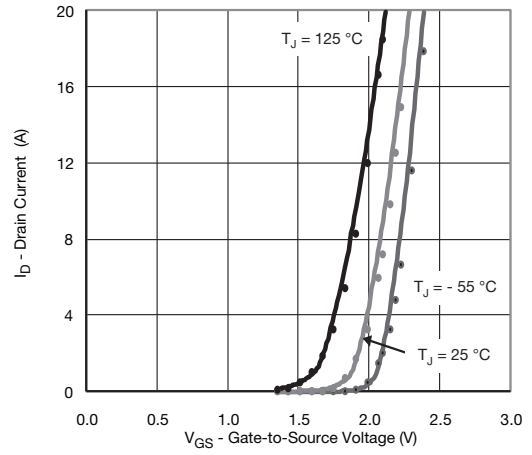
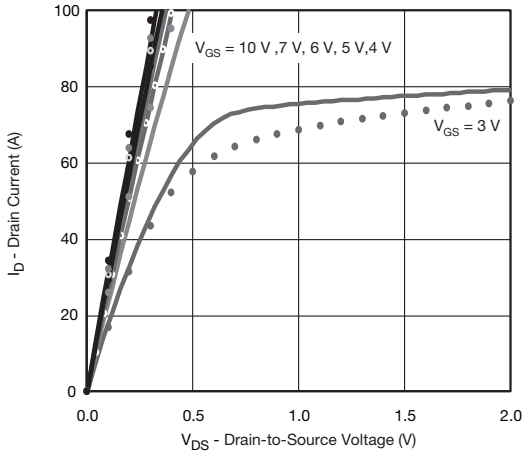
Note

Dots and squares represent measured data.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Channel 2



Note

Dots and squares represent measured data.



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