

Dual N-Channel 30 V (D-S) MOSFET

DESCRIPTION

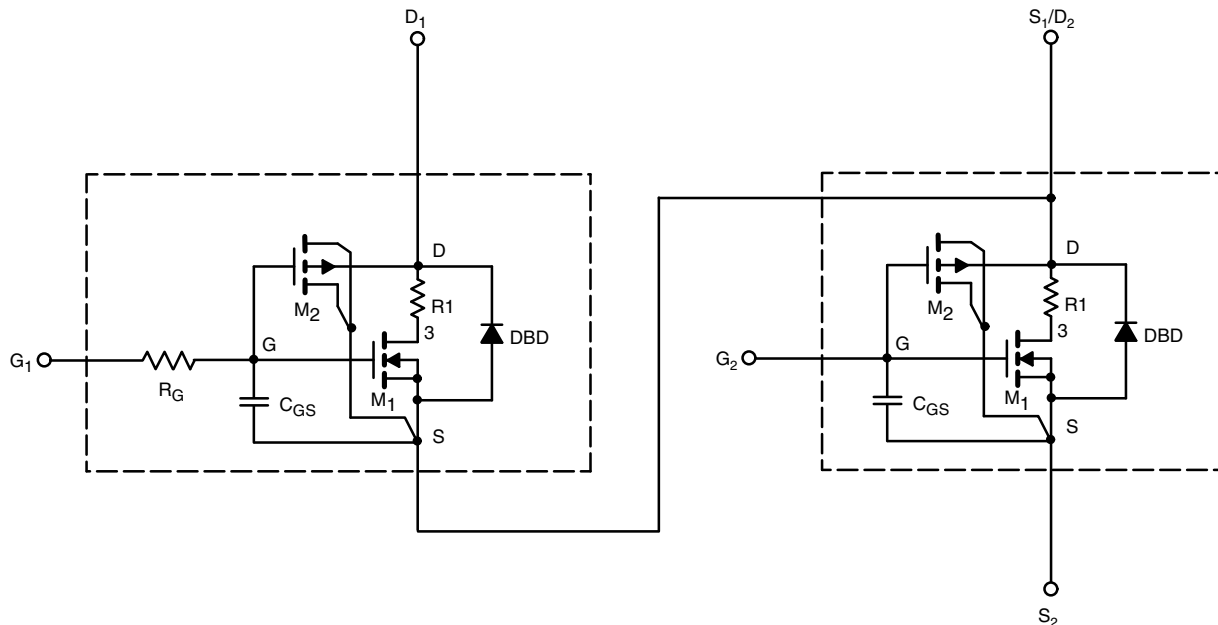
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



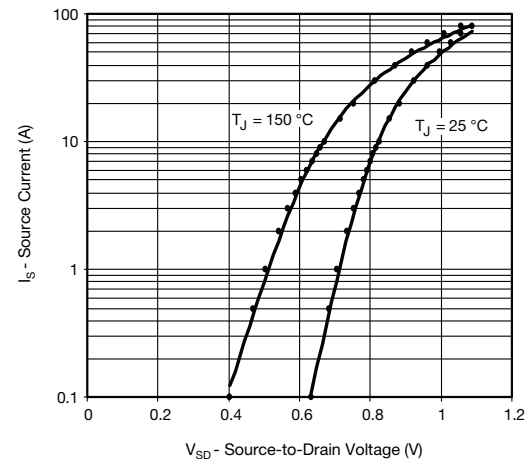
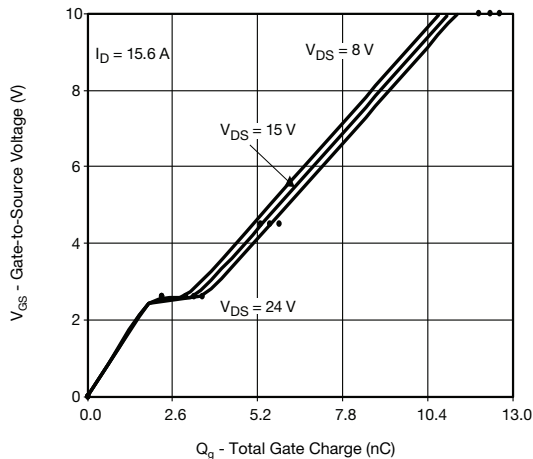
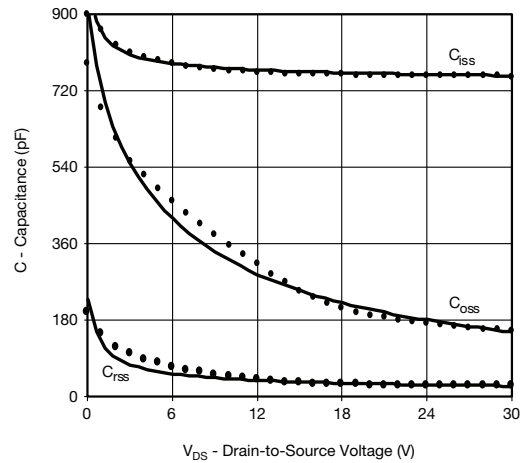
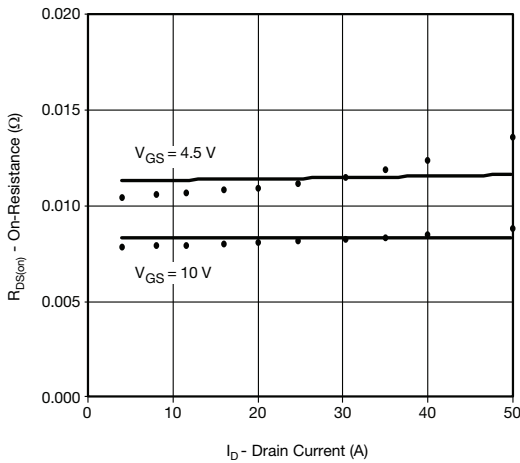
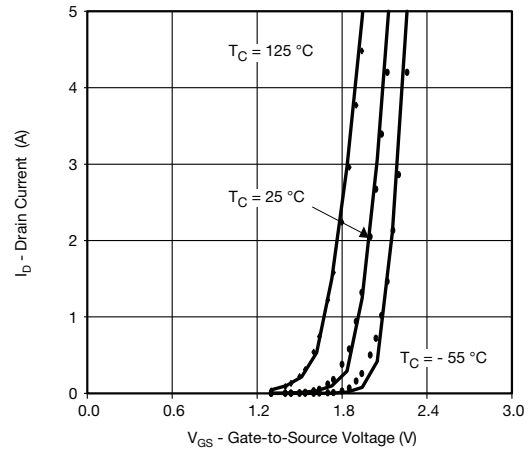
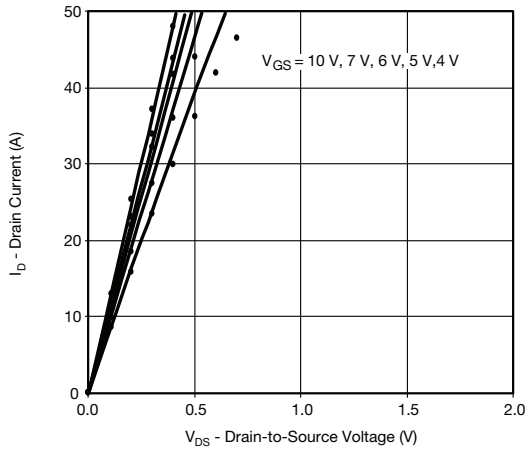
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT	
Static							
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1.5	-	V	
			Ch-2	1.8	-		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15.6 A	Ch-1	0.0083	0.0079	Ω	
			Ch-2	0.0043	0.0042		
			V _{GS} = 4.5 V, I _D = 13 A	Ch-1	0.0110		0.0110
				Ch-2	0.0061		0.0058
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 15.6 A	Ch-1	47	37	S	
		V _{DS} = 15 V, I _D = 20 A	Ch-2	65	60		
Diode Forward Voltage ^a	V _{SD}	I _S = 10 A	Ch-1	0.80	0.80	V	
			Ch-2	0.80	0.82		
Dynamic ^b							
Input Capacitance	C _{iss}	N-Channel V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	764	760	pF	
			Ch-2	1560	1552		
Output Capacitance	C _{oss}		Ch-1	249	250		
			Ch-2	450	450		
Reverse Transfer Capacitance	C _{rss}		Ch-1	33	32		
			Ch-2	42	40		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 15.6 A	Ch-1	11	12.3	nC	
		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A	Ch-2	21	22.6		
		Channel-1	Ch-1	5.6	5.6		
			Ch-2	10	10.1		
Gate-Source Charge	Q _{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 15.6 A	Ch-1	2.3	2.3		
			Ch-2	4.2	4.2		
Gate-Drain Charge	Q _{gd}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A	Ch-1	1	1		
			Ch-2	1.8	1.8		

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



CHANNEL-1 COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

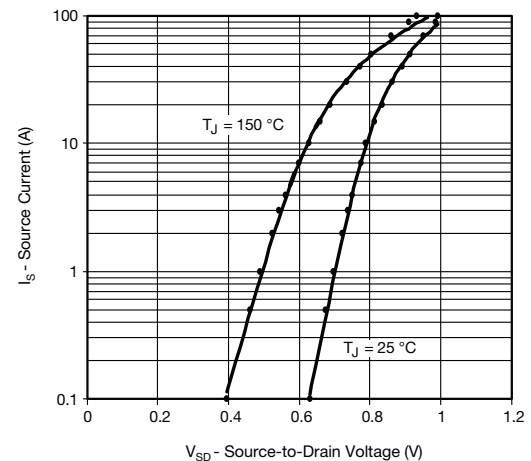
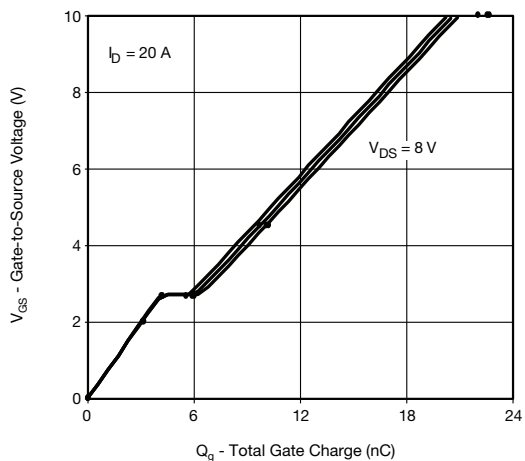
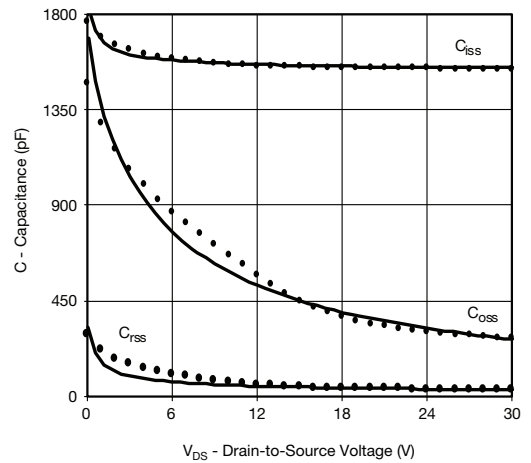
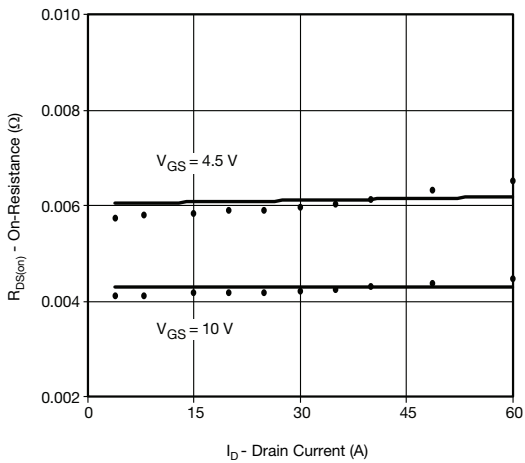
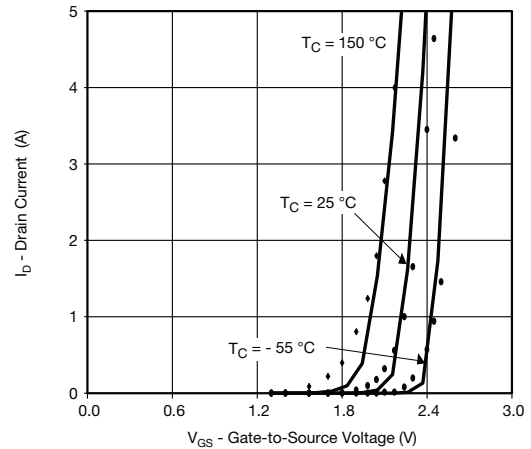
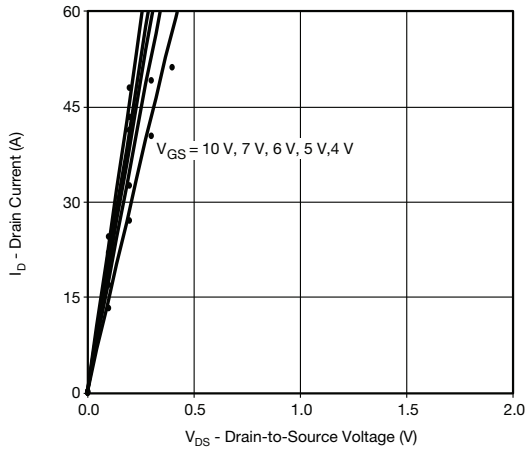


Note

- Dots and squares represent measured data.



CHANNEL-2 COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.

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