Complementary (N- and P-Channel) MOSFET

DESCRIPTION

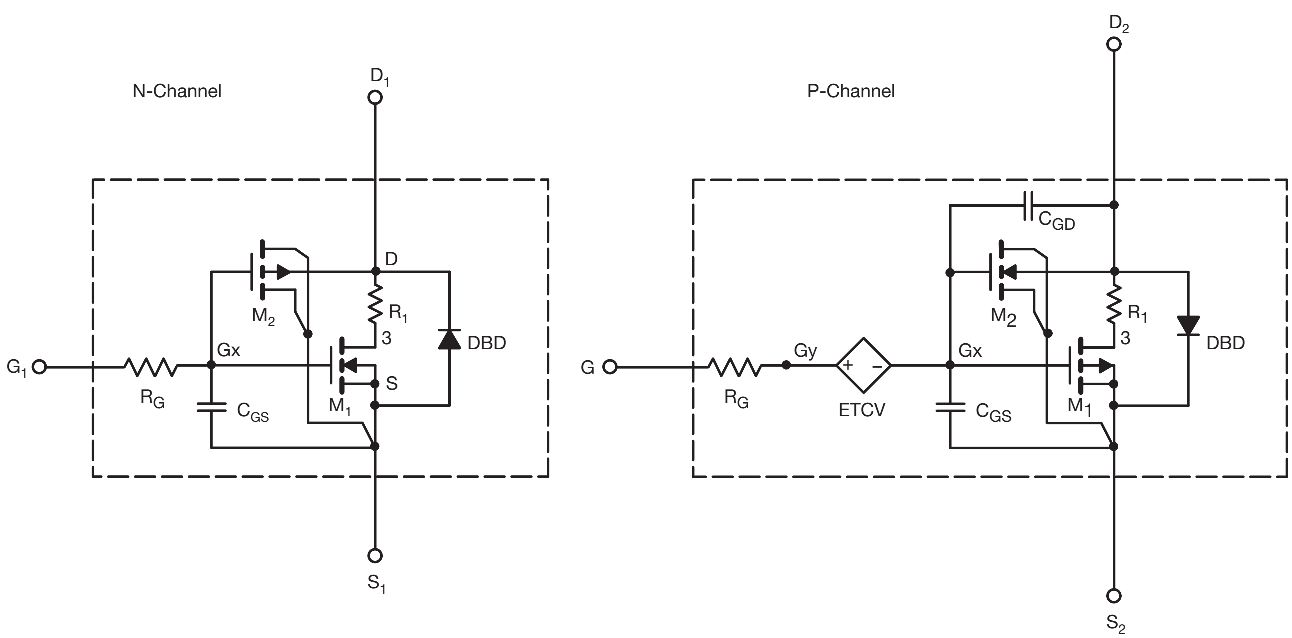
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

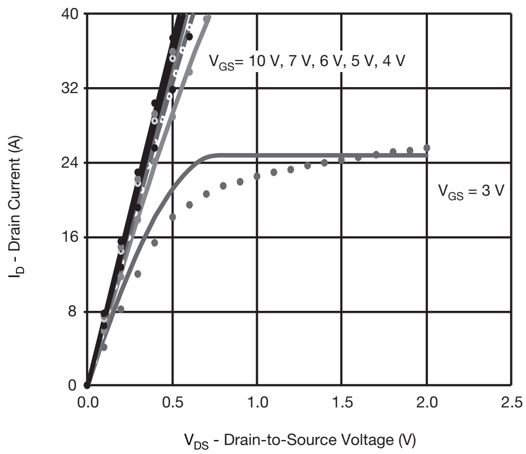
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	1.1	-	V
		$V_{DS} = V_{GS}$, I_D = - 250 µA	P-Ch	0.6	-	
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	N-Ch	0.0135	0.0135	Ω
		V_{GS} = - 10 V, I_D = - 6 A	P-Ch	0.021	0.021	
		V_{GS} = 4.5 V, I_D = 7 A	N-Ch	0.015	0.016	
		V_{GS} = - 4.5 V, I_D = - 5 A	P-Ch	0.029	0.029	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 10 A	N-Ch	23	29	S
		V_{DS} = - 15 V, I_D = - 6 A	P-Ch	21	24	
Diode Forward Voltage[a]	V_{SD}	I_S = 2 A, V_{GS} = 0 V	N-Ch	0.76	0.72	V
		I_S = - 2 A, V_{GS} = 0 V	P-Ch	- 0.70	- 0.71	
Dynamic[b]						
Input Capacitance	C_{iss}	N-Channel V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz; P-Channel V_{DS} = - 4 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	787	805	pF
			P-Ch	1420	1400	
Output Capacitance	C_{oss}		N-Ch	174	170	
			P-Ch	636	660	
Reverse Transfer Capacitance	C_{rss}		N-Ch	80	80	
			P-Ch	610	630	
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 10 A	N-Ch	14	16.5	nC
		V_{DS} = - 4 V, V_{GS} = - 10 V, I_D = - 6 A	P-Ch	28	27.5	
		N-Channel V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A; P-Channel V_{DS} = - 4 V, V_{GS} = - 4.5 V, I_D = - 6 A	N-Ch	7.1	7.9	
			P-Ch	14	16.5	
Gate-Source Charge	Q_{gs}		N-Ch	2.2	2.2	
			P-Ch	2.2	2.2	
Gate-Drain Charge	Q_{gd}		N-Ch	2.7	2.7	
			P-Ch	4.8	4.8	

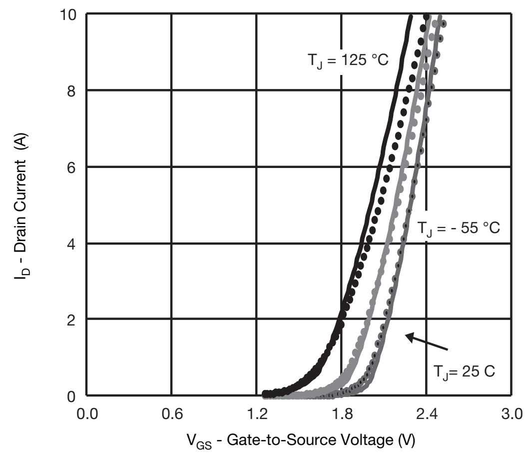
Notes

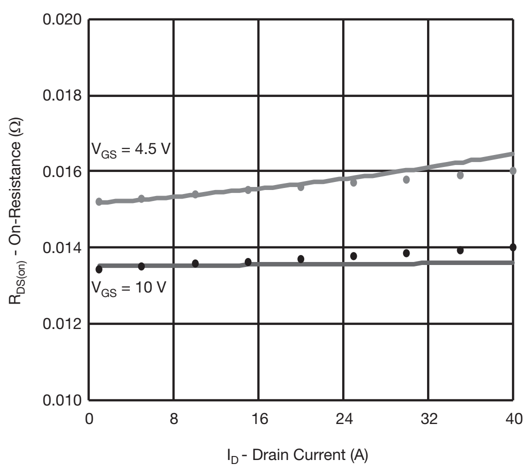
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

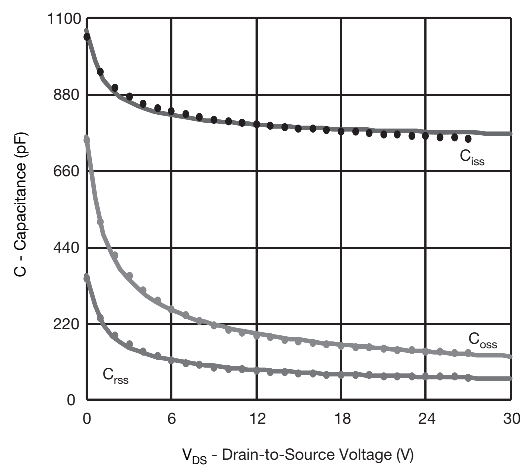
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

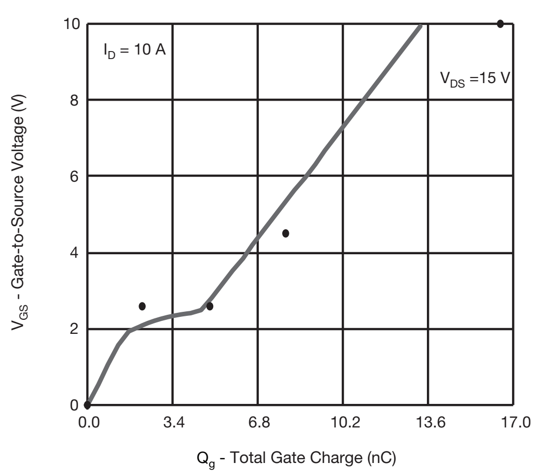
N-Channel MOSFET

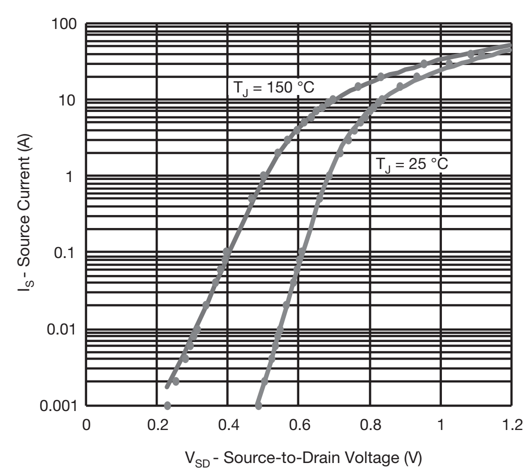










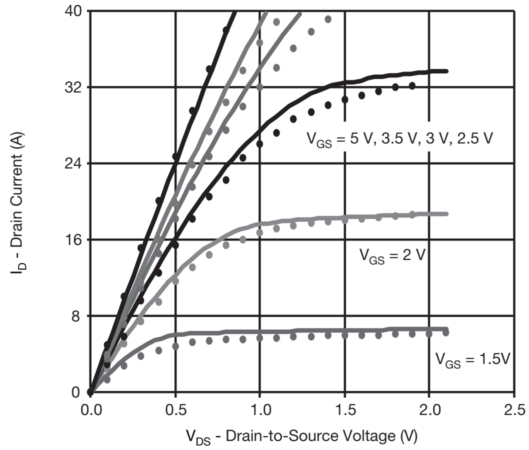


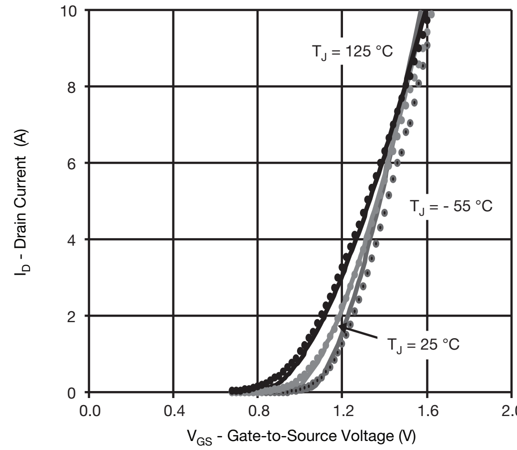
Note

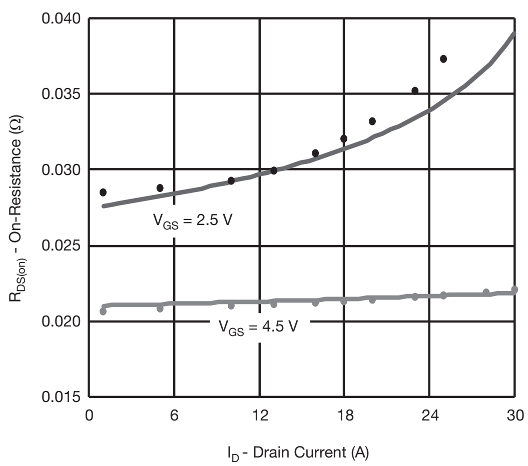
- Dots and squares represent measured data.

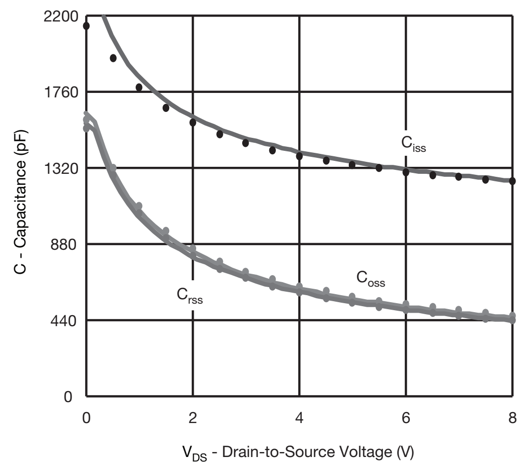
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

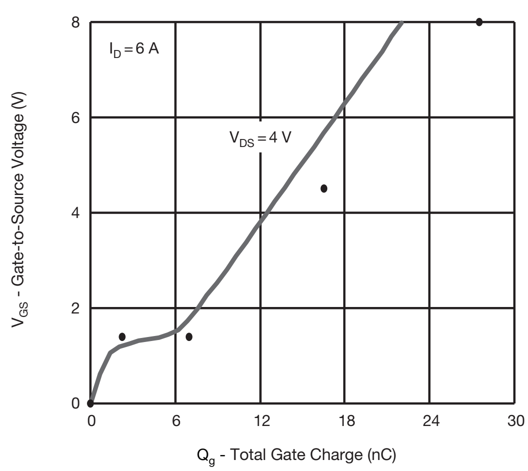
P-Channel MOSFET

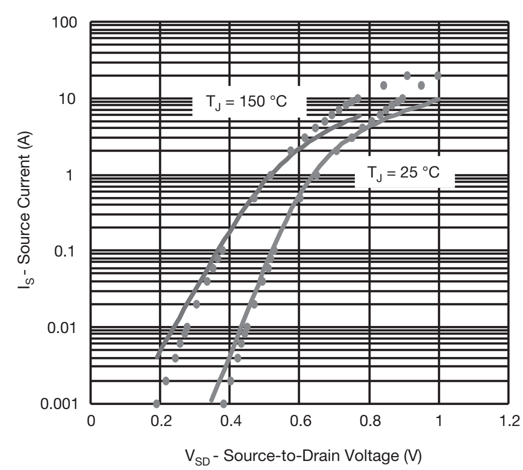












Note

- Dots and squares represent measured data.

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