

Dual N-Channel 30 V (D-S) MOSFET

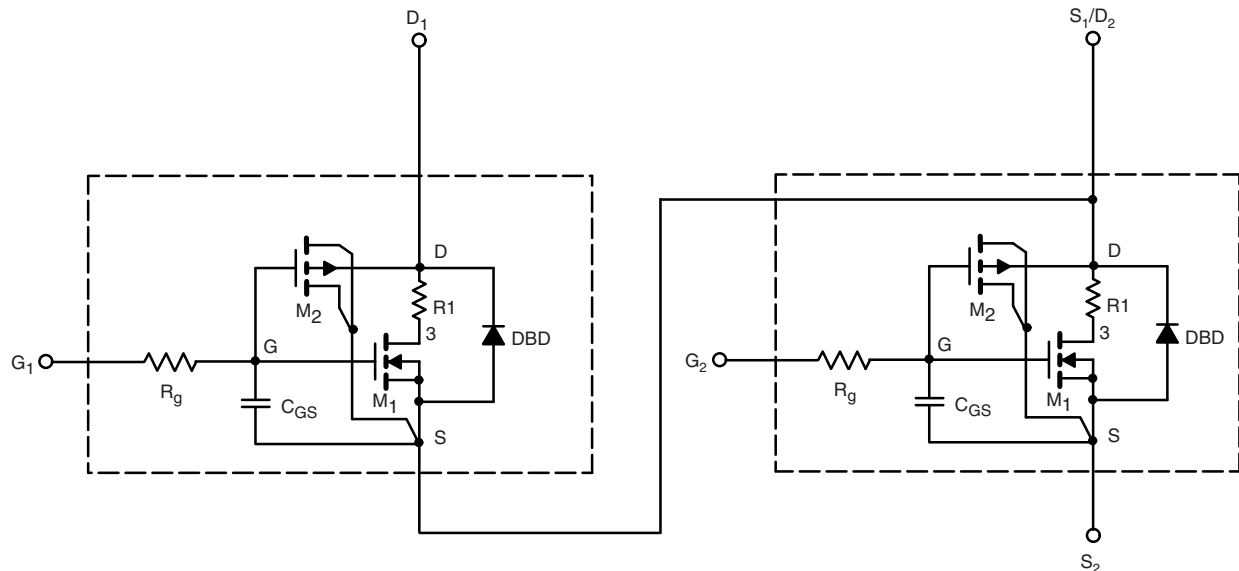
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1.7	-	V
			Ch-2	1.7	-	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7.8\text{ A}$	Ch-1	0.018	0.020	Ω
			Ch-2	0.0103	0.0105	
			Ch-1	0.023	0.024	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 7.8\text{ A}$	Ch-1	19	17	S
			Ch-2	32	24	
Diode Forward Voltage ^a	V_{SD}	$I_S = 6.3\text{ A}$	Ch-1	0.83	0.80	V
			Ch-2	1.65	1.78	
Dynamic^b						
Input Capacitance	C_{iss}	Channel 1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	Ch-1	413	435	pF
			Ch-2	845	846	
Output Capacitance	C_{oss}	Channel 2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	Ch-1	88	95	
			Ch-2	190	187	
Reverse Transfer Capacitance	C_{rss}	Channel 1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	Ch-1	45	42	
			Ch-2	76	72	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 7.8\text{ A}$	Ch-1	8	8	nC
			Ch-2	14	15.4	
		Channel 1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.8\text{ A}$	Ch-1	4.2	3.8	
			Ch-2	7	7.3	
Gate-Source Charge	Q_{gs}	Channel 2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1	1.4	1.4	
			Ch-2	2.3	2.3	
Gate-Drain Charge	Q_{gd}	Channel 2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1	1.1	1.1	
			Ch-2	2.2	2.2	

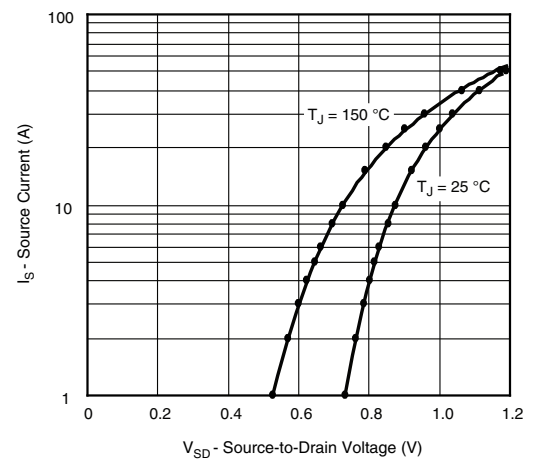
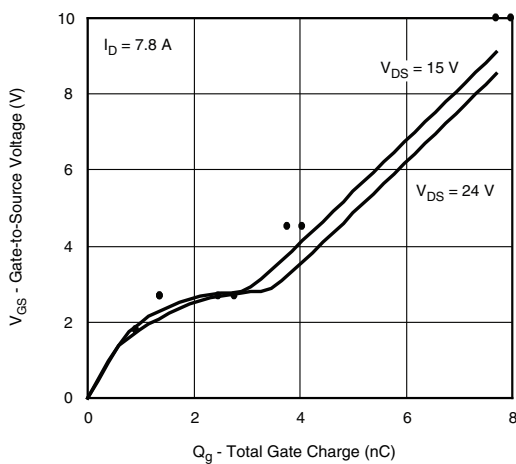
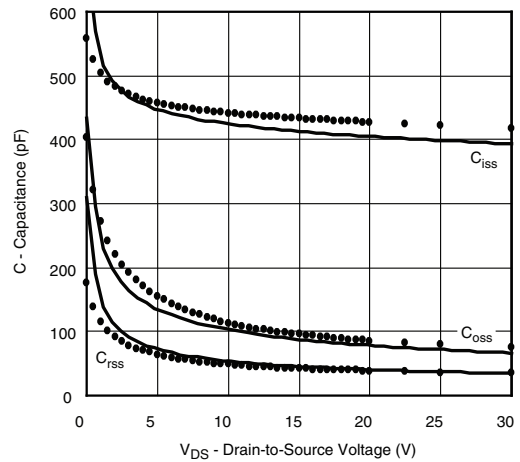
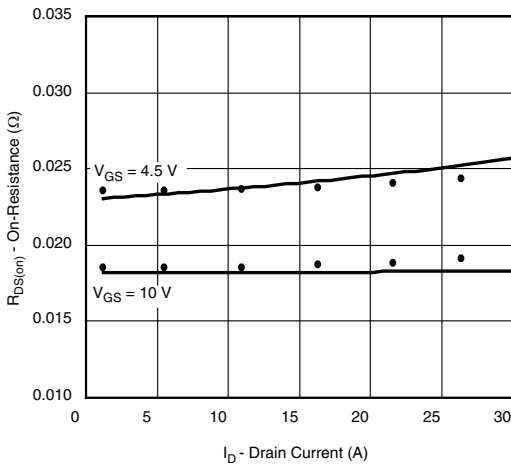
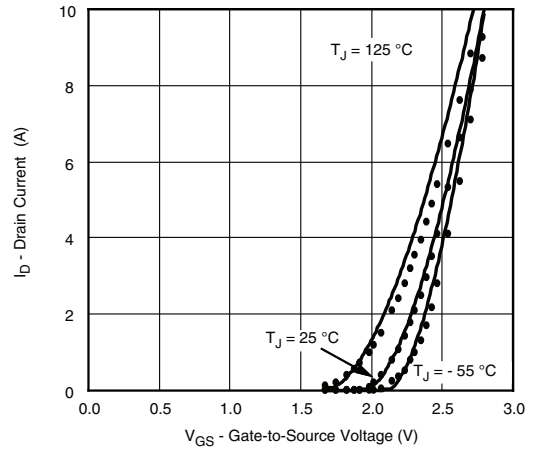
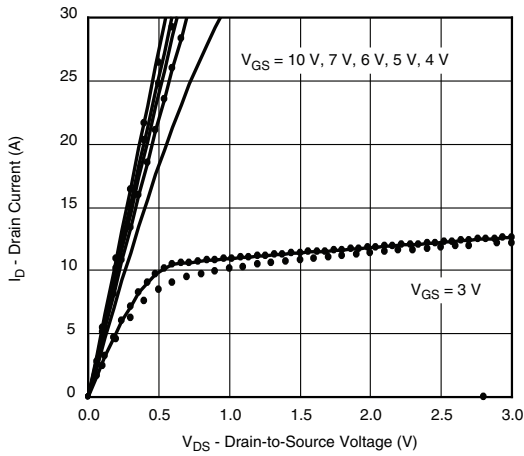
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Channel 1



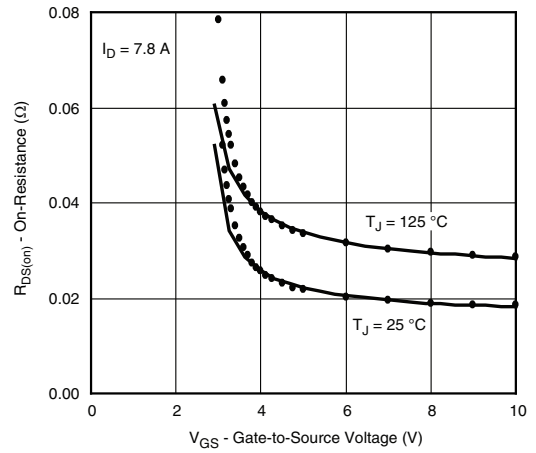
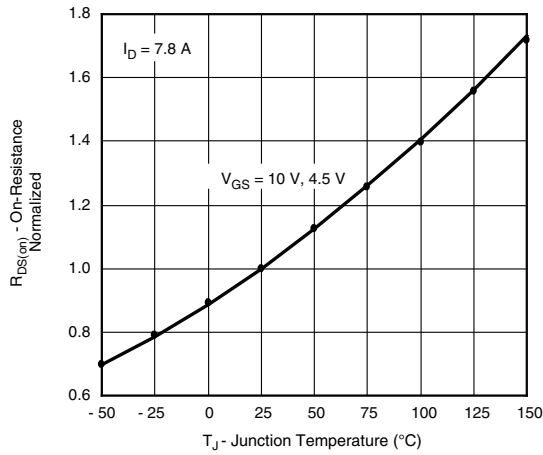
Note

- Dots and squares represent measured data.



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Channel 1



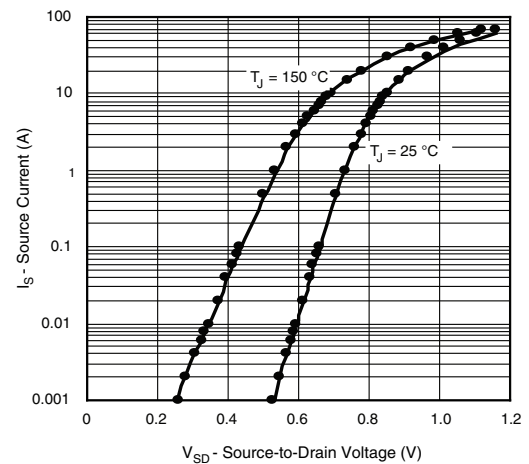
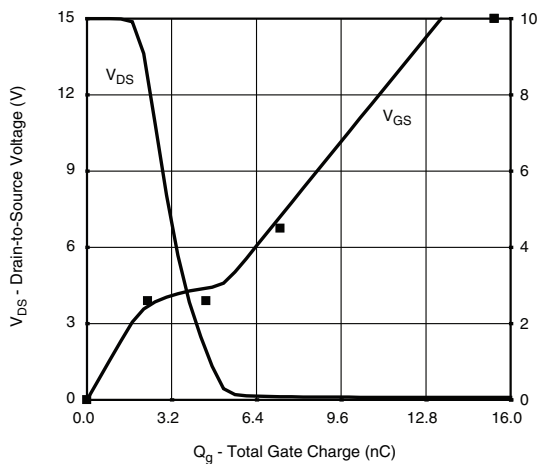
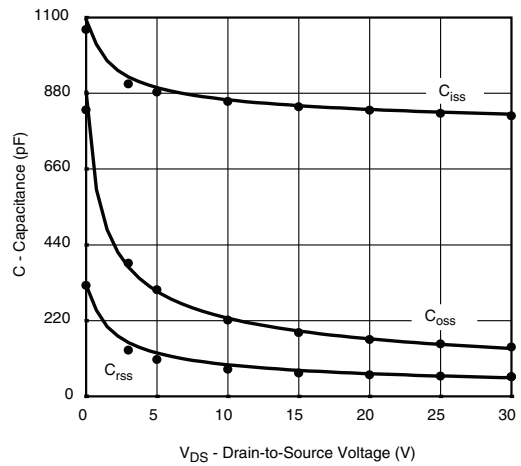
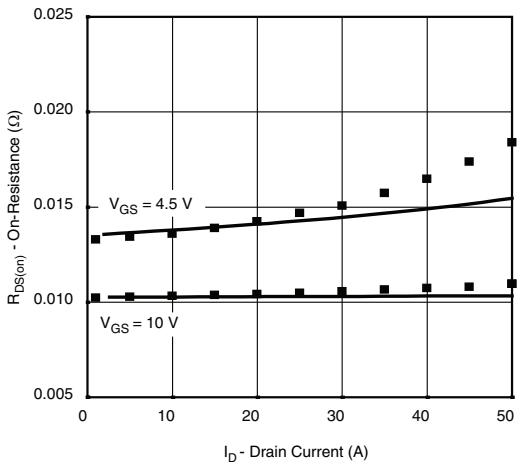
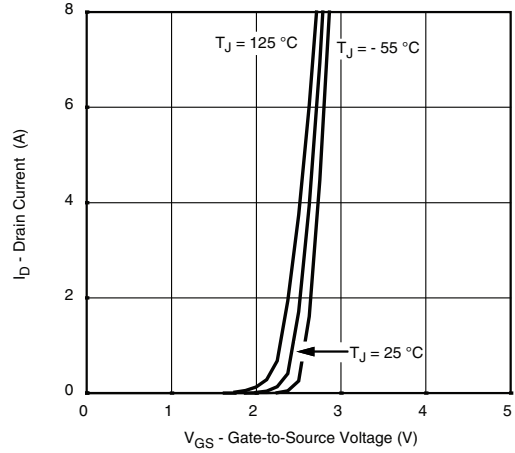
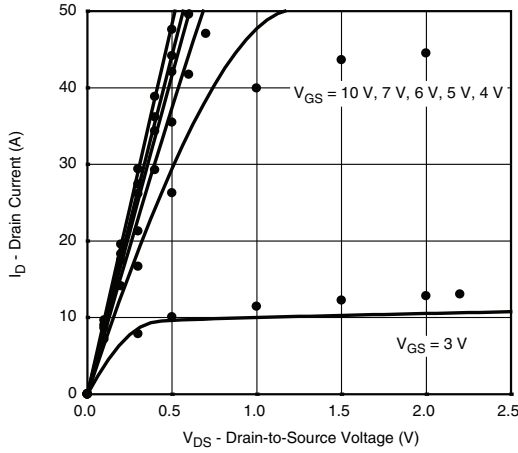
Note

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COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Channel 2



Note

- Dots and squares represent measured data.



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