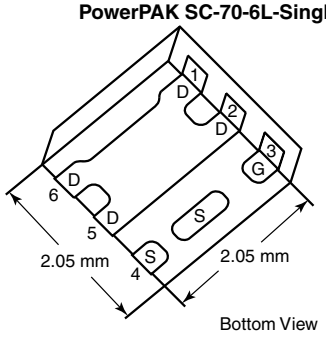
# N-Channel 100 V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) Max. | $I_D$ (A)[a] | $Q_g$ (Typ.) |
| 100 | 0.083 at $V_{GS}$ = 10 V | 11.3 | 3.5 nC |
| | 0.130 at $V_{GS}$ = 4.5 V | 9 | |

**PowerPAK SC-70-6L-Single**




Bottom View

**Ordering Information:**
SiA416DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

## FEATURES

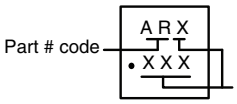
- TrenchFET® Power MOSFET
- 100 % $R_g$ and UIS Tested
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

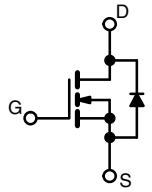
Pb-free
RoHS COMPLIANT
HALOGEN FREE

## APPLICATIONS

- DC/DC Converters
- Full-Bridge Converters
- For Power Bricks and POL Power

**Marking Code**




N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted) | | | | |
|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Limit** | **Unit** |
| Drain-Source Voltage | | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $T_C$ = 25 °C | $I_D$ | 11.3 | A |
| | $T_C$ = 70 °C | | 9 | |
| | $T_A$ = 25 °C | | 4.8[b, c] | |
| | $T_A$ = 70 °C | | 3.9[b, c] | |
| Pulsed Drain Current (t = 300 µs) | | $I_{DM}$ | 15 | |
| Continuous Source-Drain Diode Current | $T_C$ = 25 °C | $I_S$ | 12 | |
| | $T_A$ = 25 °C | | 2.9[b, c] | |
| Single Pulse Avalanche Current | L = 0.1 mH | $I_{AS}$ | 3 | |
| Single Pulse Avalanche Energy | | $E_{AS}$ | 0.45 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | $P_D$ | 19 | W |
| | $T_C$ = 70 °C | | 12 | |
| | $T_A$ = 25 °C | | 3.5[b, c] | |
| | $T_A$ = 70 °C | | 2.2[b, c] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to 150 | °C |
| Soldering Recommendations (Peak Temperature)[d, e] | | | 260 | |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Typical** | **Maximum** | **Unit** |
| Maximum Junction-to-Ambient[b, f] | t ≤ 5 s | $R_{thJA}$ | 28 | 36 | °C/W |
| Maximum Junction-to-Case (Drain) | Steady State | $R_{thJC}$ | 5.3 | 6.5 | |

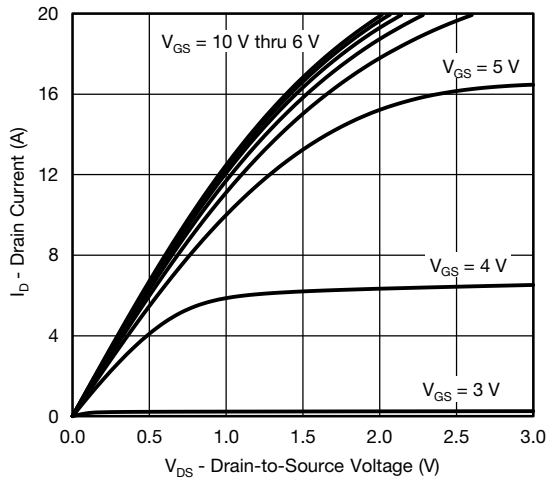
Notes:
a. Based on $T_C$ = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 80 °C/W.

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 100 | | | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = 250 µA | | 54 | | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | | - 4.4 | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1.6 | | 3 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | | | 10 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS} \geq$ 5 V, $V_{GS}$ = 10 V | 10 | | | A |
| Drain-Source On-State Resistance[a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 3.2 A | | 0.068 | 0.083 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 2.6 A | | 0.092 | 0.130 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 3.2 A | | 8 | | S |
| **Dynamic[b]** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1 MHz | | 295 | | pF |
| Output Capacitance | $C_{oss}$ | | | 92 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 16 | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 50 V, $V_{GS}$ = 10 V, $I_D$ = 4.8 A | | 6.5 | 10 | nC |
| | | $V_{DS}$ = 50 V, $V_{GS}$ = 4.5 V, $I_D$ = 4.8 A | | 3.5 | 5.3 | |
| Gate-Source Charge | $Q_{gs}$ | | | 1.2 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 1.9 | | |
| Output Charge | $Q_{oss}$ | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 7.6 | | |
| Gate Resistance | $R_g$ | f = 1 MHz | 0.4 | 1.8 | 3.6 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 50 V, $R_L$ = 12.8 Ω<br>$I_D \cong$ 3.9 A, $V_{GEN}$ = 10 V, $R_g$ = 1 Ω | | 5 | 10 | ns |
| Rise Time | $t_r$ | | | 13 | 25 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 10 | 20 | |
| Fall Time | $t_f$ | | | 10 | 20 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 50 V, $R_L$ = 12.8 Ω<br>$I_D \cong$ 3.9 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 Ω | | 25 | 50 | |
| Rise Time | $t_r$ | | | 100 | 200 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 15 | 30 | |
| Fall Time | $t_f$ | | | 25 | 50 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | $T_C$ = 25 °C | | | 12 | A |
| Pulse Diode Forward Current[a] | $I_{SM}$ | | | | 15 | |
| Body Diode Voltage | $V_{SD}$ | $I_S$ = 3.9 A | | 0.85 | 1.2 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = 3.9 A, dI/dt = 100 A/µs, $T_J$ = 25 °C | | 30 | 60 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | 30 | 60 | nC |
| Reverse Recovery Fall Time | $t_a$ | | | 20 | | ns |
| Reverse Recovery Rise Time | $t_b$ | | | 10 | | |

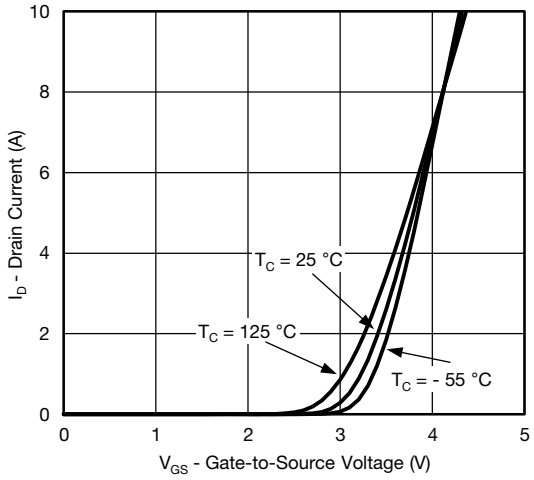
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

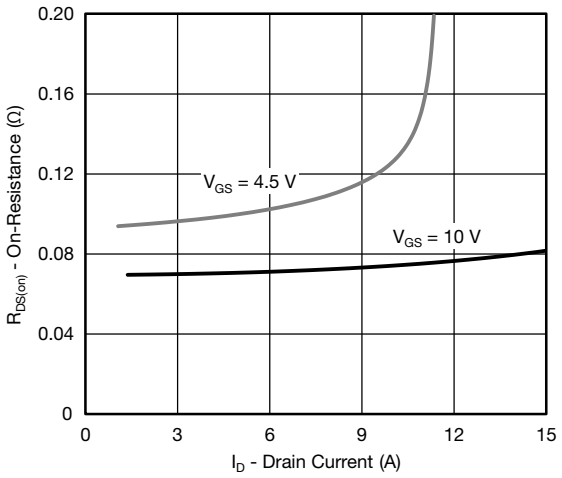
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



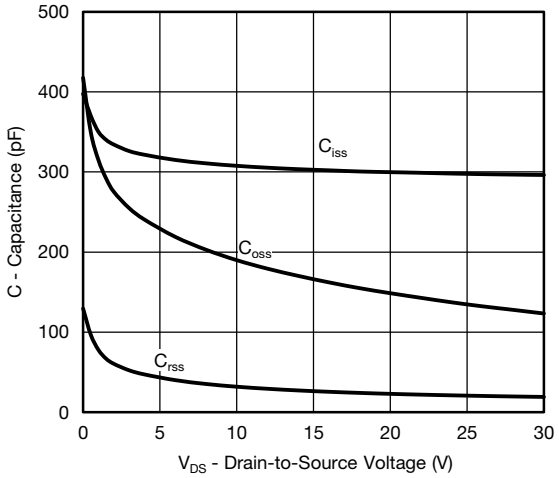

**Output Characteristics**



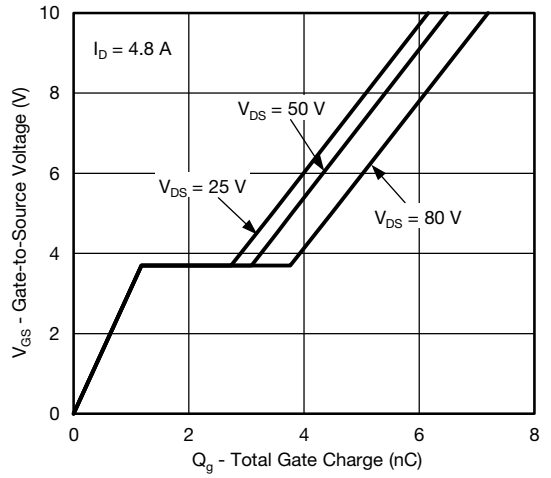

**Transfer Characteristics**



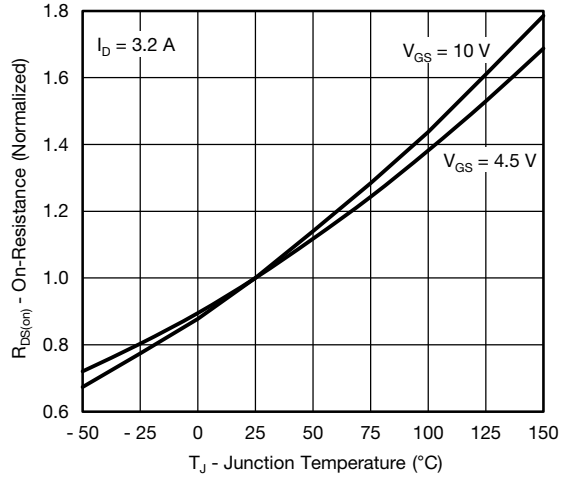

**On-Resistance vs. Drain Current and Gate Voltage**




**Capacitance**

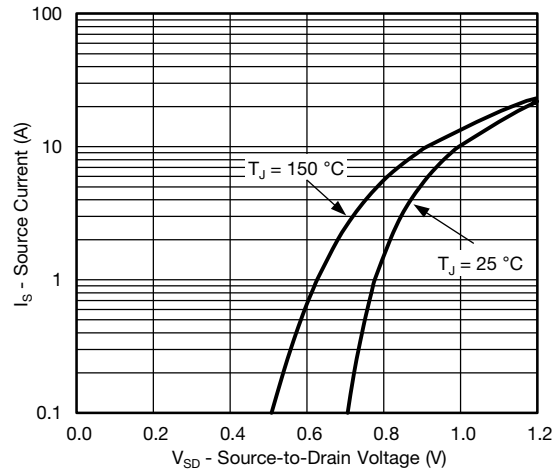



**Gate Charge**

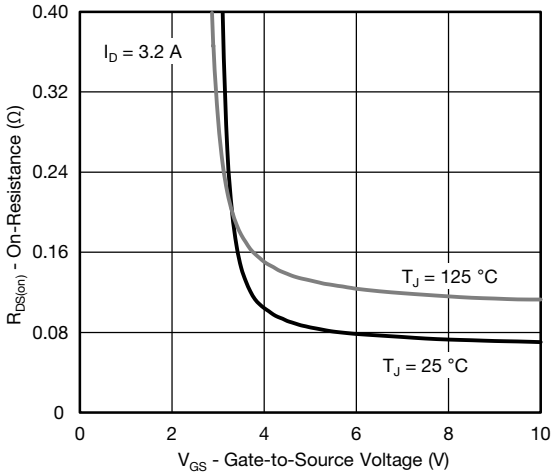



**On-Resistance vs. Junction Temperature**

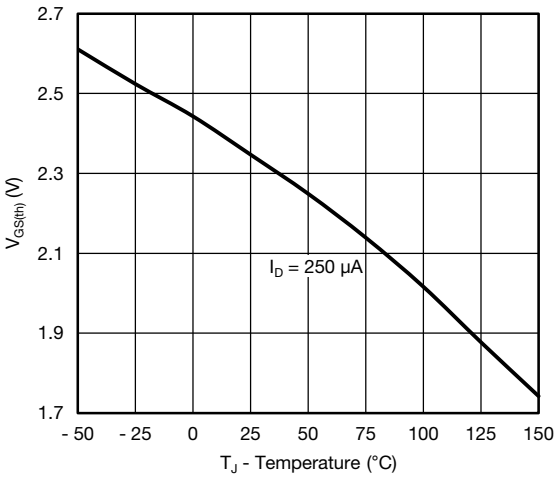
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



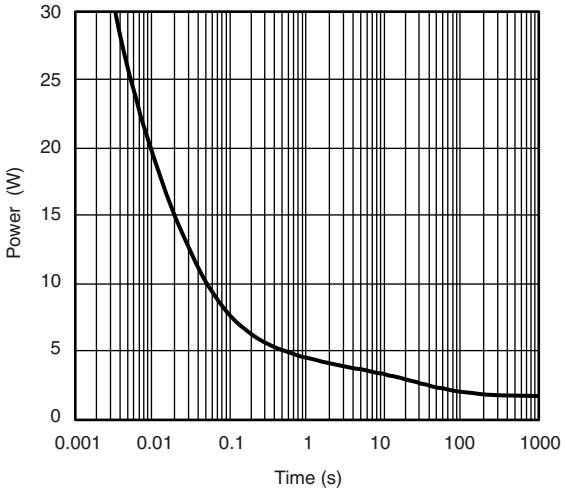

**Source-Drain Diode Forward Voltage**



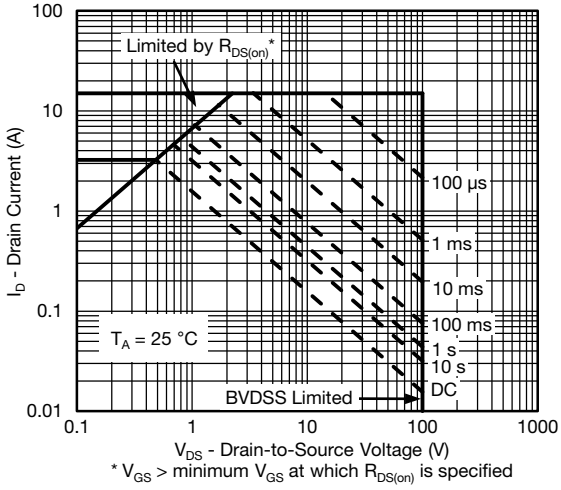

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**




**Single Pulse Power, Junction-to-Ambient**

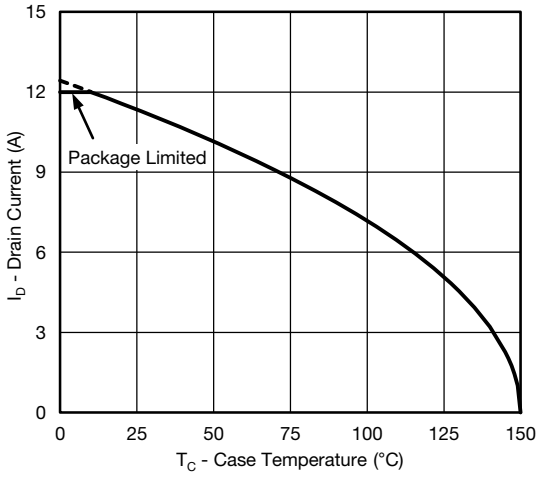



**Safe Operating Area, Junction-to-Ambient**

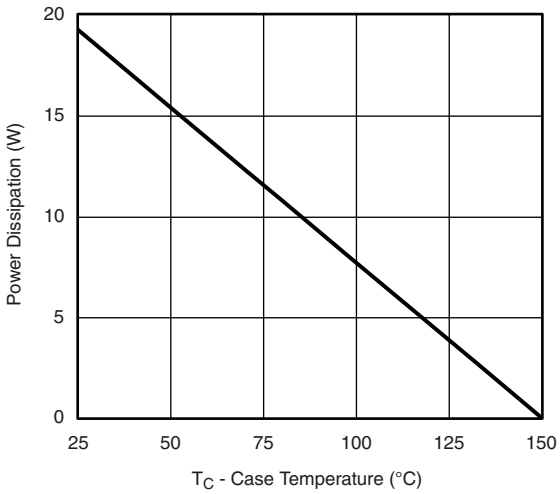

For technical questions, contact: pmostechsupport@vishay.com

Document Number: 63649
S12-2438-Rev. B, 15-Oct-12

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



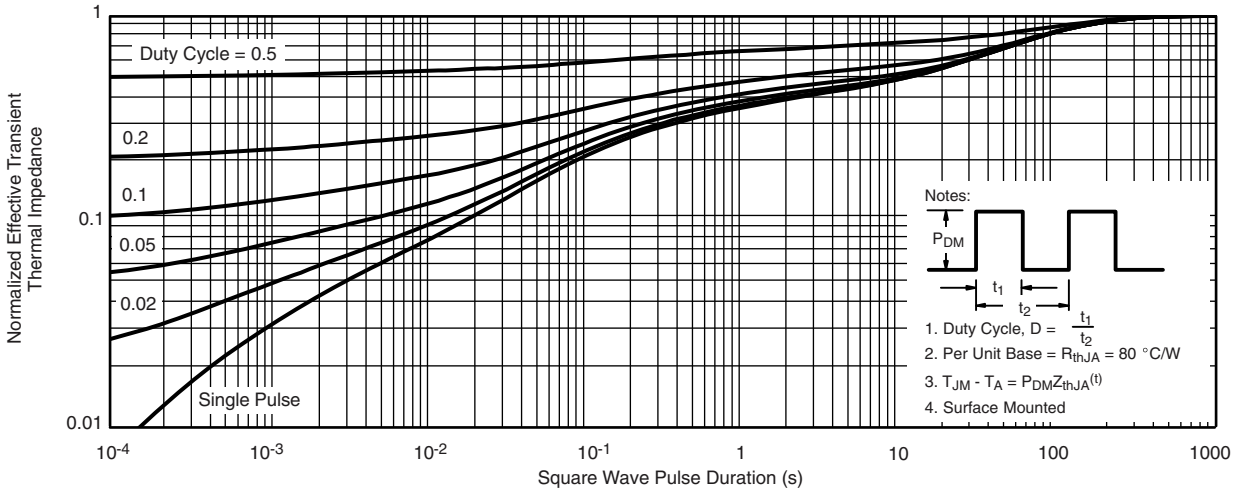

**Current Derating***



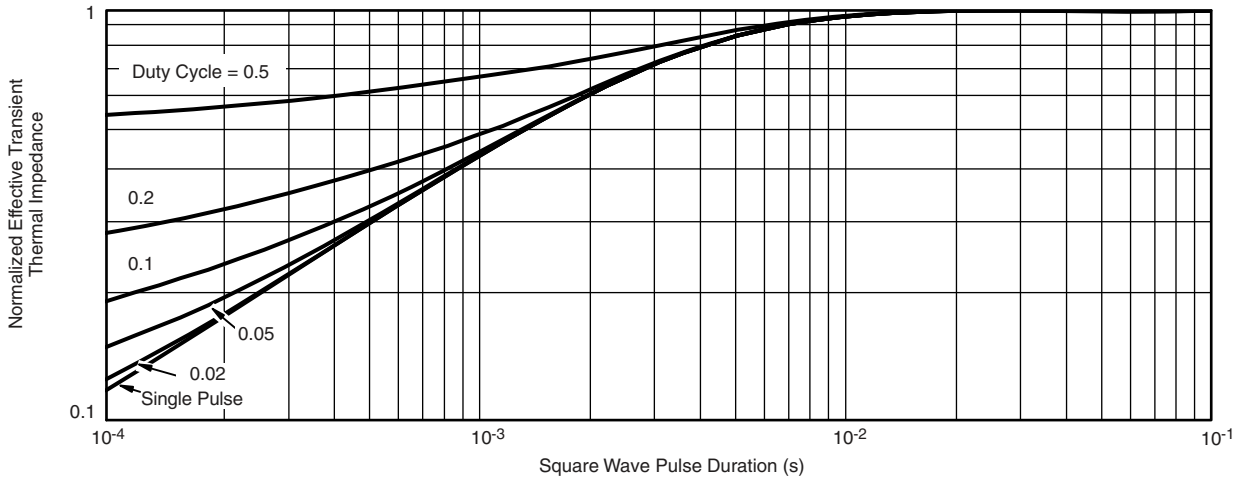

**Power, Junction-to-Case**

* The power dissipation $P_D$ is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



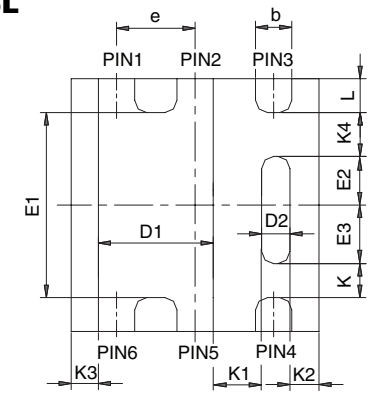

**Normalized Thermal Transient Impedance, Junction-to-Ambient**



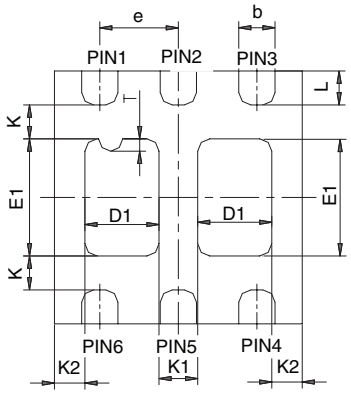

**Normalized Thermal Transient Impedance, Junction-to-Case**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63649.*

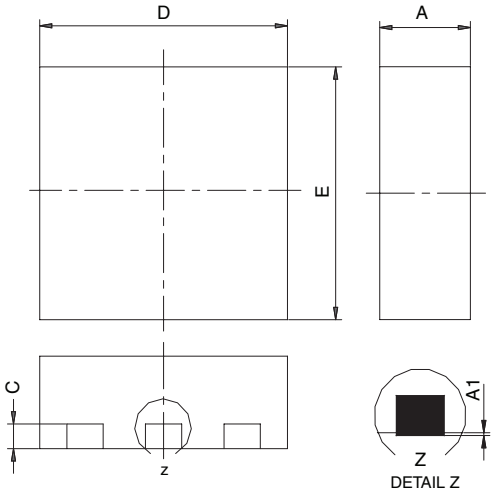
## PowerPAK® SC70-6L




BACKSIDE VIEW OF SINGLE




BACKSIDE VIEW OF DUAL



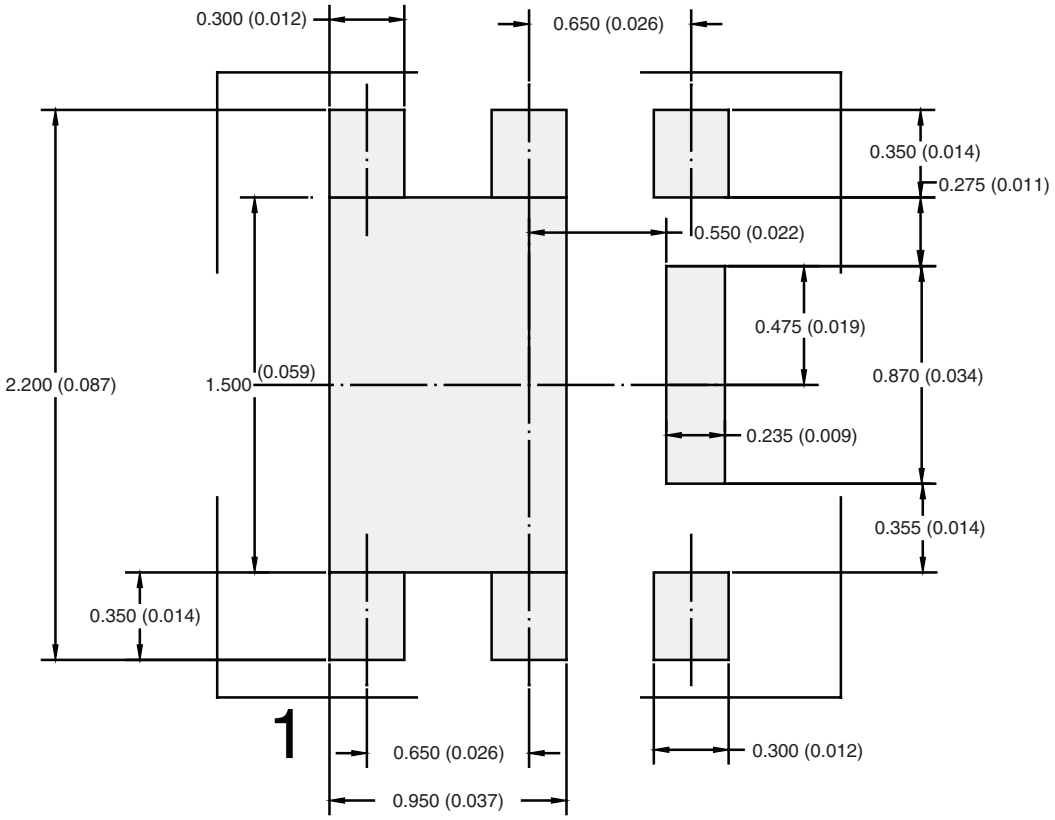

DETAIL Z

Notes:
1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

| DIM | SINGLE PAD | | | | | | DUAL PAD | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MILLIMETERS | | | INCHES | | | MILLIMETERS | | | INCHES | | |
| | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max |
| A | 0.675 | 0.75 | 0.80 | 0.027 | 0.030 | 0.032 | 0.675 | 0.75 | 0.80 | 0.027 | 0.030 | 0.032 |
| A1 | 0 | - | 0.05 | 0 | - | 0.002 | 0 | - | 0.05 | 0 | - | 0.002 |
| b | 0.23 | 0.30 | 0.38 | 0.009 | 0.012 | 0.015 | 0.23 | 0.30 | 0.38 | 0.009 | 0.012 | 0.015 |
| C | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 1.98 | 2.05 | 2.15 | 0.078 | 0.081 | 0.085 | 1.98 | 2.05 | 2.15 | 0.078 | 0.081 | 0.085 |
| D1 | 0.85 | 0.95 | 1.05 | 0.033 | 0.037 | 0.041 | 0.513 | 0.613 | 0.713 | 0.020 | 0.024 | 0.028 |
| D2 | 0.135 | 0.235 | 0.335 | 0.005 | 0.009 | 0.013 | | | | | | |
| E | 1.98 | 2.05 | 2.15 | 0.078 | 0.081 | 0.085 | 1.98 | 2.05 | 2.15 | 0.078 | 0.081 | 0.085 |
| E1 | 1.40 | 1.50 | 1.60 | 0.055 | 0.059 | 0.063 | 0.85 | 0.95 | 1.05 | 0.033 | 0.037 | 0.041 |
| E2 | 0.345 | 0.395 | 0.445 | 0.014 | 0.016 | 0.018 | | | | | | |
| E3 | 0.425 | 0.475 | 0.525 | 0.017 | 0.019 | 0.021 | | | | | | |
| e | 0.65 BSC | | | 0.026 BSC | | | 0.65 BSC | | | 0.026 BSC | | |
| K | 0.275 TYP | | | 0.011 TYP | | | 0.275 TYP | | | 0.011 TYP | | |
| K1 | 0.400 TYP | | | 0.016 TYP | | | 0.320 TYP | | | 0.013 TYP | | |
| K2 | 0.240 TYP | | | 0.009 TYP | | | 0.252 TYP | | | 0.010 TYP | | |
| K3 | 0.225 TYP | | | 0.009 TYP | | | | | | | | |
| K4 | 0.355 TYP | | | 0.014 TYP | | | | | | | | |
| L | 0.175 | 0.275 | 0.375 | 0.007 | 0.011 | 0.015 | 0.175 | 0.275 | 0.375 | 0.007 | 0.011 | 0.015 |
| T | | | | | | | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5934

**RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single**




Dimensions in mm/(Inches)

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