

N- and P-Channel 30 V (D-S) MOSFET

DESCRIPTION

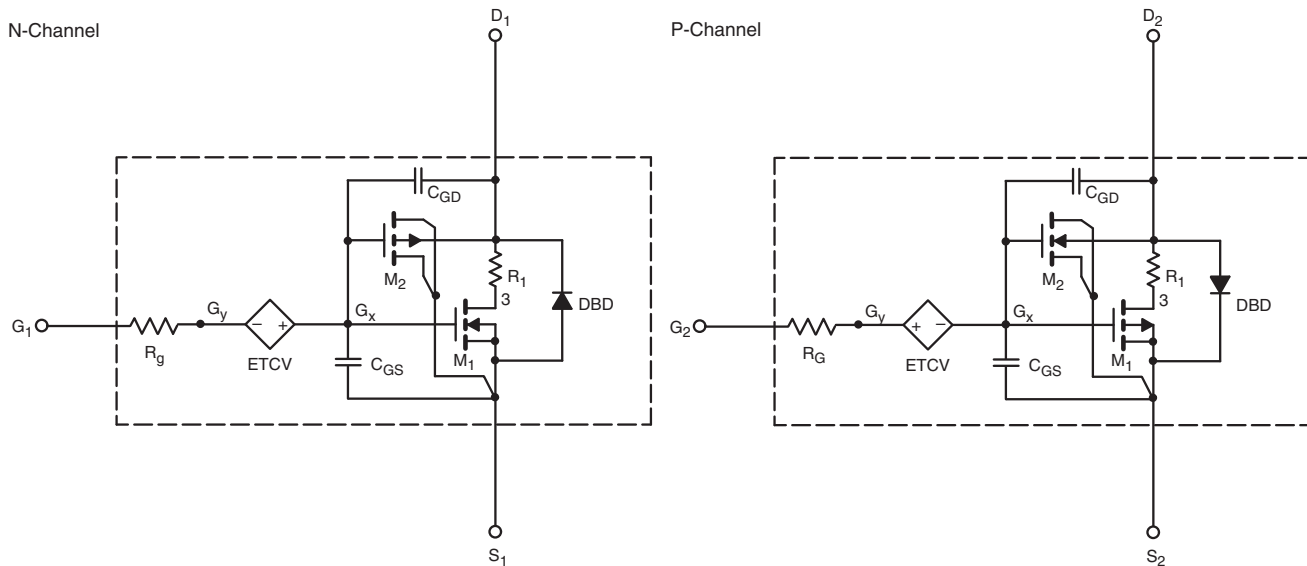
The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	2	-	V
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	2.4	-	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 0.6 A	N-Ch	0.322	0.323	Ω
		V _{GS} = - 10 V, I _D = - 0.4 A	P-Ch	0.740	0.740	
		V _{GS} = 4.5V, I _D = 0.1 A	N-Ch	0.458	0.437	
		V _{GS} = - 4.5 V, I _D = - 0.1 A	P-Ch	1.4	1.4	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 0.6 A	N-Ch	1.4	1.2	S
		V _{DS} = - 15 V, I _D = - 0.4 A	P-Ch	0.71	0.60	
Diode Forward Voltage ^a	V _{SD}	I _S = 0.5 A, V _{GS} = 0 V	N-Ch	0.86	0.80	V
		I _S = - 0.4 A, V _{GS} = 0 V	P-Ch	- 0.89	- 0.80	
Dynamic^b						
Input Capacitance	C _{iss}	N-Channel V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	28	28	pF
			P-Ch	34	34	
Output Capacitance	C _{oss}		N-Ch	10	10	
			P-Ch	12	12	
Reverse Transfer Capacitance	C _{rss}		N-Ch	5	5	
			P-Ch	7	7	
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 0.6 A	N-Ch	0.53	1	nC
		V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 0.4 A	P-Ch	0.72	1.5	
		N-Channel V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 0.6 A	N-Ch	0.29	0.55	
			P-Ch	0.40	0.80	
Gate-Source Charge	Q _{gs}	P-Channel V _{DS} = - 15 V, V _{GS} = - 4.5 V, I _D = - 0.4 A	N-Ch	0.20	0.20	
			P-Ch	0.40	0.40	
Gate-Drain Charge	Q _{gd}	N-Ch	0.20	0.20		
		P-Ch	0.35	0.35		

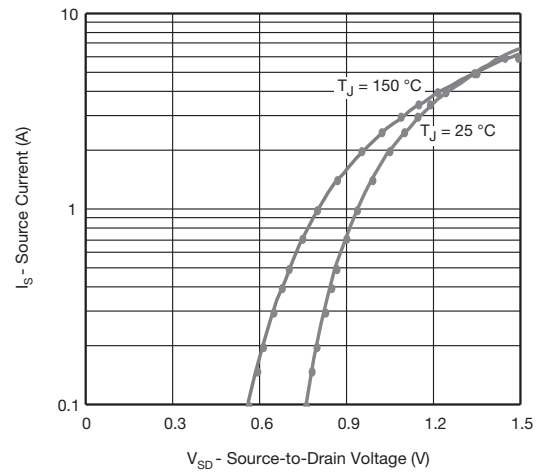
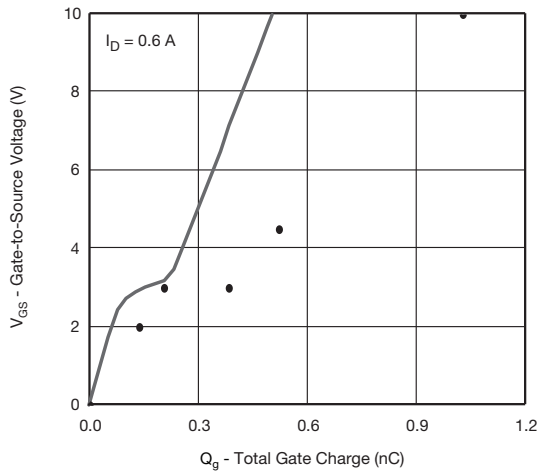
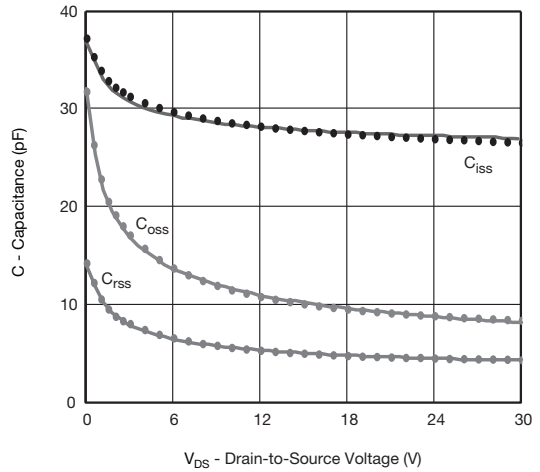
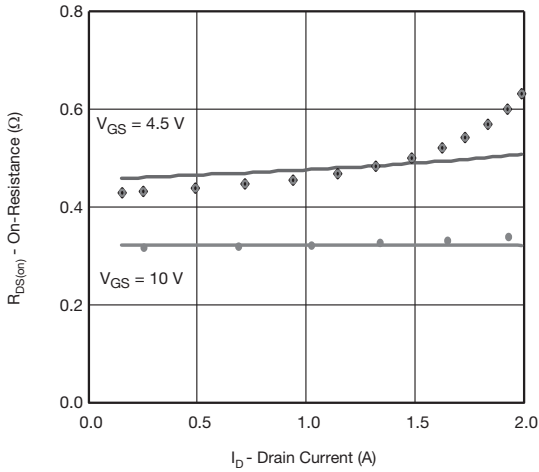
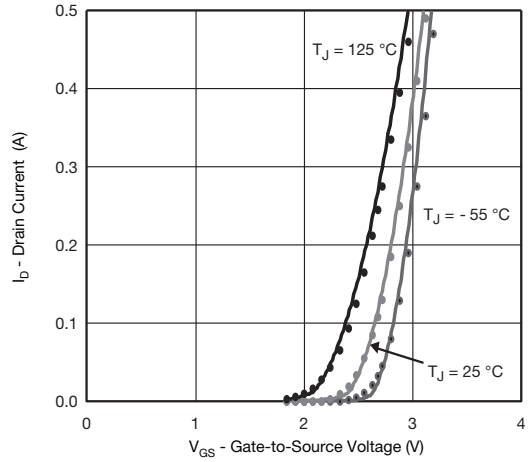
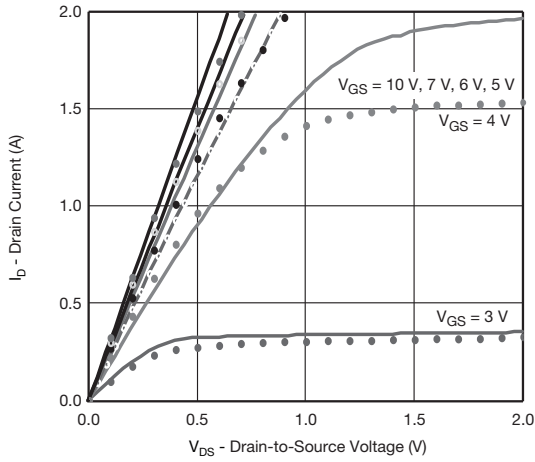
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

N-Channel MOSFET



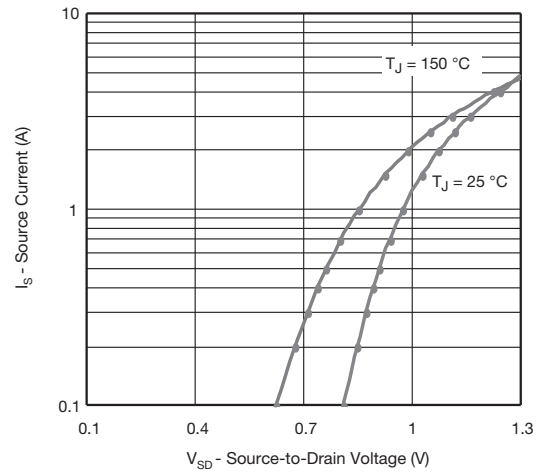
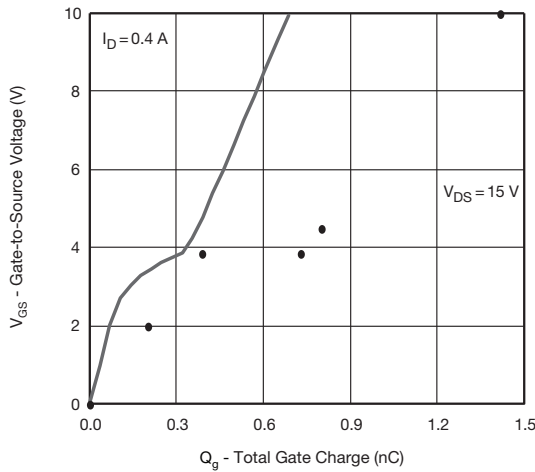
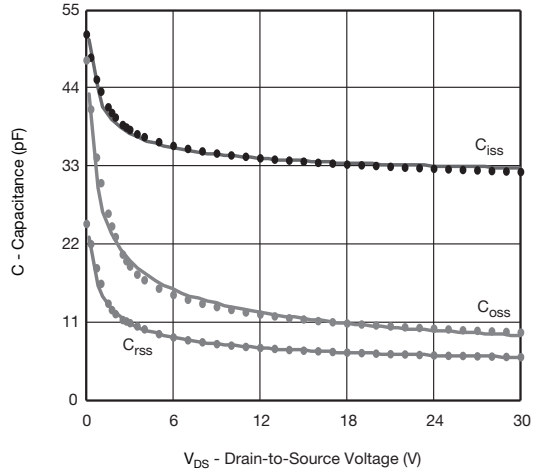
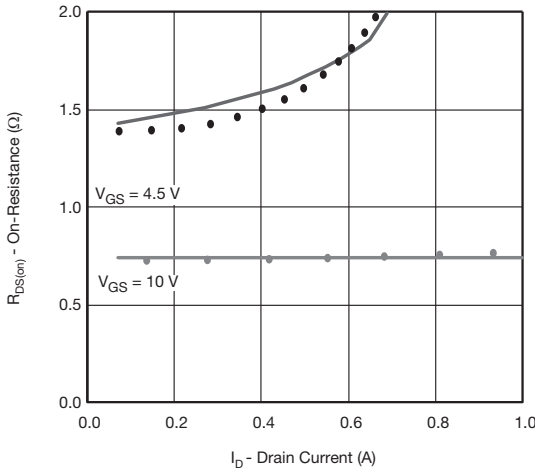
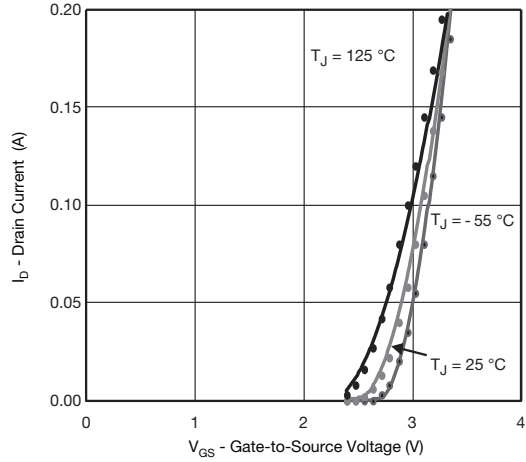
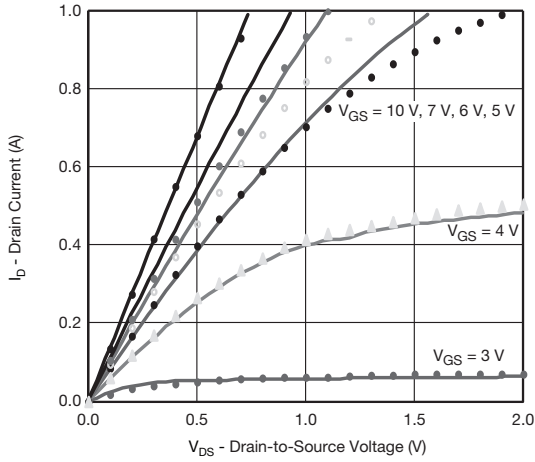
Note

- Dots and squares represent measured data.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

P-Channel MOSFET



Note

- Dots and squares represent measured data.



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