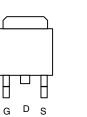
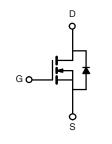


# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	40			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 V$	0.0017			
I <sub>D</sub> (A)	120			
Configuration	Single			

TO-263





Top View

N-Channel MOSFET

#### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualified<sup>d</sup>
- 100 %  $\rm R_g$  and UIS Tested
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>



ORDERING INFORMATION		
Package	TO-263	
Lead (Pb)-free and Halogen-free	SQM120N04-1m7-GE3	

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25 \degree C$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	40	
Gate-Source Voltage		V <sub>GS</sub>	± 20	V
Continuous Drain Current <sup>a</sup>	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	120	A
Continuous Drain Current.	T <sub>C</sub> = 125 °C		120	
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	120	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	480	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	85	
Single Pulse Avalanche Energy		E <sub>AS</sub>	361	mJ
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	- P <sub>D</sub>	375	W
	T <sub>C</sub> = 125 °C		125	vv
Operating Junction and Storage Temperature Ra	nge	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient P	CB Mount <sup>c</sup>	R <sub>thJA</sub>	40	°C/W
Junction-to-Case (Drain)		R <sub>thJC</sub>	0.4	0/10

Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

c. When mounted on 1" square PCB (FR-4 material).

d. Parametric verification ongoing.

# SQM120N04-1m7



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static					1			
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		40	-	-	v	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	· V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5	3.0	3.5	v	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, $V_{GS} = \pm 20 V$	-	-	± 100	nA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V	-	-	1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	120	-	-	Α	
		$V_{GS} = 10 V$	I <sub>D</sub> = 30 A	-	0.0014	0.0017	Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C	-	-	0.0027		
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C	-	-	0.0033	1	
Forward Transconductance <sup>b</sup>	<b>g</b> fs	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 30 A	-	198	-	S	
Dynamic <sup>b</sup>					•			
Input Capacitance	C <sub>iss</sub>			-	13 880	17 350	pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 25 V, f = 1 MHz	-	5720	7150		
Reverse Transfer Capacitance	C <sub>rss</sub>	1		-	840	1050		
Total Gate Charge <sup>c</sup>	Qg			-	206	310		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 V$	$V_{DS} = 20 \text{ V}, \text{ I}_{D} = 120 \text{ A}$	-	50	-	nC	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>				44	-		
Gate Resistance	Rg	f = 1 MHz		0.57	1.14	1.71	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	$\label{eq:VDD} \begin{array}{l} V_{DD} = 20 \text{ V}, \text{ R}_L = 0.17 \ \Omega \\ \text{I}_D \cong 120 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_g = 1 \ \Omega \end{array}$		-	26	39		
Rise Time <sup>c</sup>	t <sub>r</sub>			-	21	32	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	68	102		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	12	18		
Source-Drain Diode Ratings and Characteristics <sup>b</sup>								
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	480	Α	
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 80 A, V <sub>GS</sub> = 0		-	0.86	1.5	V	

Notes

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

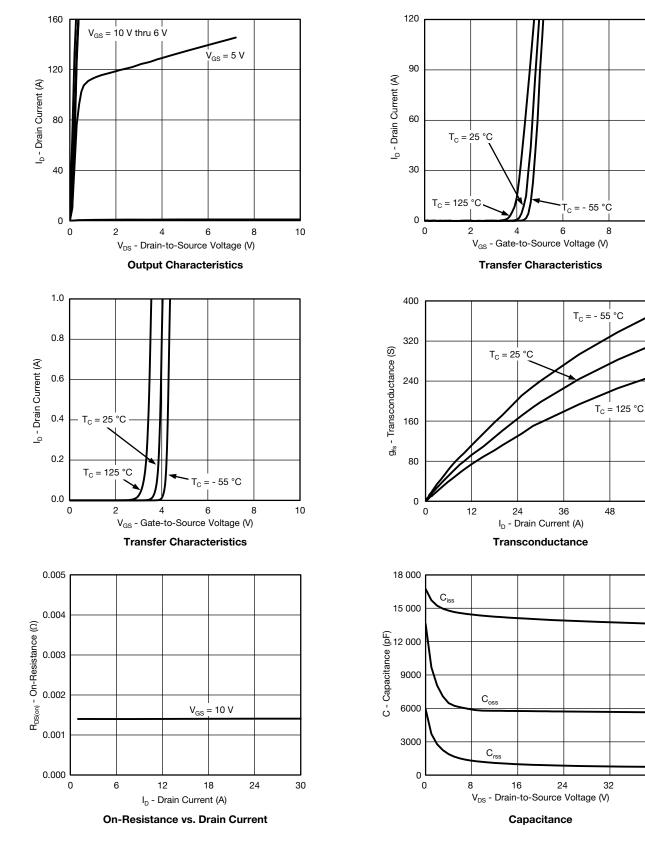
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



10

60

### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



S12-0532-Rev. A, 12-Mar-12

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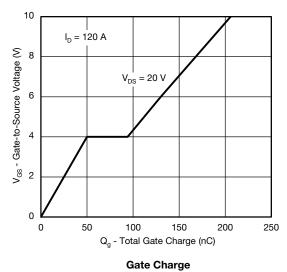
40

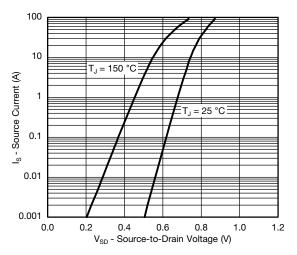
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SQM120N04-1m7

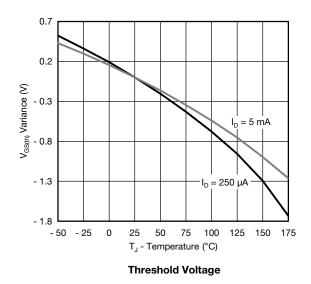
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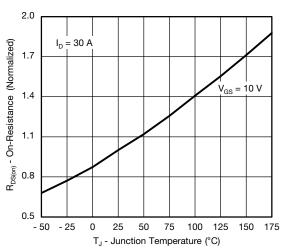
## **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



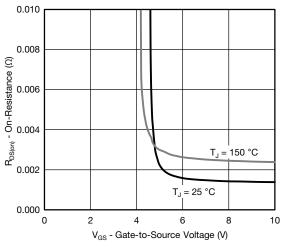


Source Drain Diode Forward Voltage

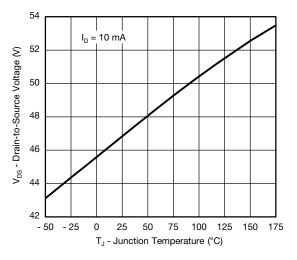




**On-Resistance vs. Junction Temperature** 



**On-Resistance vs. Gate-to-Source Voltage** 



Drain Source Breakdown vs. Junction Temperature

S12-0532-Rev. A, 12-Mar-12

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Document Number: 63811

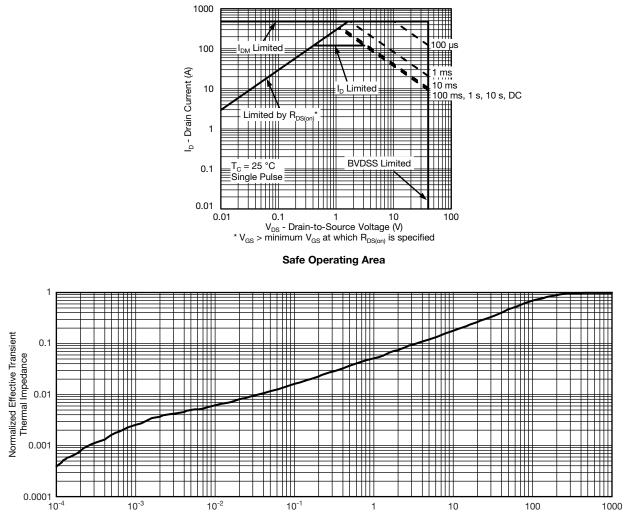
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# SQM120N04-1m7



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### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



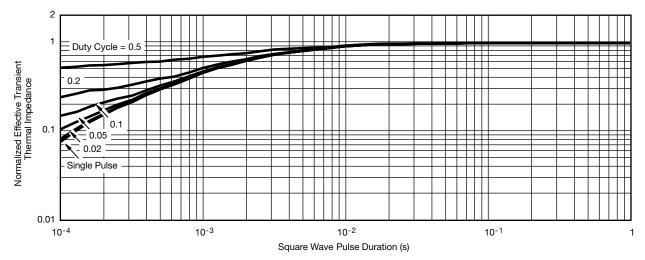
Square Wave Pulse Duration (s)

Normalized Thermal Transient Impedance, Junction-to-Ambient





### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction to Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction to Case (25 °C)

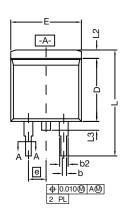
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

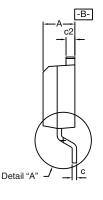
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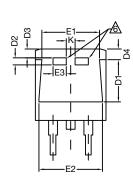


TO-263 (D<sup>2</sup>PAK): 3-LEAD

#### VERSION 1: FACILITY CODE = T

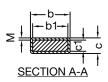








DETAIL A (ROTATED 90°)



		INCHES		MILLIMETERS	
DIM.		MIN.	MAX.	MIN.	MAX.
Α		0.160	0.190	4.064	4.826
	b	0.020	0.039	0.508	0.990
	b1	0.020	0.035	0.508	0.889
	b2	0.045	0.055	1.143	1.397
с*	Thin lead	0.013	0.018	0.330	0.457
C	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
CI	Thick lead	0.023	0.027	0.584	0.685
	c2	0.045	0.055	1.143	1.397
	D	0.340	0.380	8.636	9.652
	D1	0.220	0.240	5.588	6.096
	D2	0.038	0.042	0.965	1.067
	D3	0.045	0.055	1.143	1.397
	D4	0.044	0.052	1.118	1.321
	E	0.380	0.410	9.652	10.414
	E1	0.245	-	6.223	-
	E2	0.355	0.375	9.017	9.525
	E3	0.072	0.078	1.829	1.981
е		0.100 BSC		2.54 BSC	
К		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
	М	-	0.002	-	0.050

#### Notes

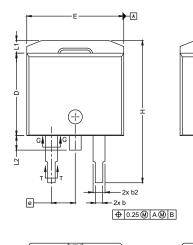
- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB.
- Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

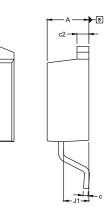
This feature is for thick lead.

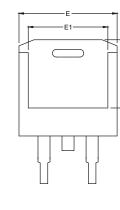
Revison: 28-Oct-2024

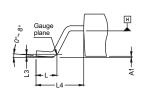


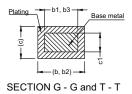
#### VERSION 2: FACILITY CODE = N











OPTION 1 2 leads



2

 $\oplus$ 

3 leads

DIM.	MIN.	MAX.		
A	4.36	4.56		
A1	0	0.25		
b	0.70	0.90		
b1	0.51	0.89		
b2	1.20	1.46		
b3	1.17	1.37		
с	0.38	0.694		
c1	0.38	0.534		
c2	1.19	1.34		
D	8.60	9.00		
D1	6.9	7.5		
E	10.15	10.55		
E1	8.1	8.7		
e	2.54 BSC			
Н	15.0	15.6		
L	1.9	2.5		
L1	-	1.65		
L2	-	1.78		
L3	0.25 typ.			
L4	4.78	5.28		
J1	2.56	2.96		
ECN: S24-1080-Rev. L, 28-Oct-2024 DWG: 5843				



### **RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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