

Vishay Siliconix

N-Channel 30 V (D-S) MOSFET

DESCRIPTION

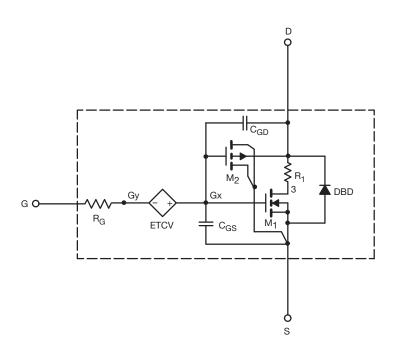
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - $55\,^{\circ}$ C to + $125\,^{\circ}$ C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPICE Device Model Si4128BDY

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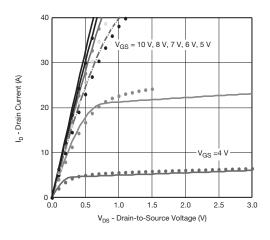
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.7	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 8.4 \text{ A}$	0.016	0.017	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$	0.026	0.027	
Forward Transconductancea	9 _{fs}	$V_{DS} = 15 \text{ V}, I_D = 8.4 \text{ A}$	16	22	S
Body Diode Voltage	V _{SD}	I _S = 6.7 A	0.86	0.85	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	403	405	pF
Output Capacitance	C _{oss}		111	110	
Reverse Transfer Capacitance	C _{rss}		57	56	
Total Gate Charge	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 8.4 \text{ A}$	6.9	7.5	nC
			3.7	3.7	
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 8.4 \text{ A}$	1.6	1.6	
Gate-Drain Charge	Q_{gd}		1.3	1.3	

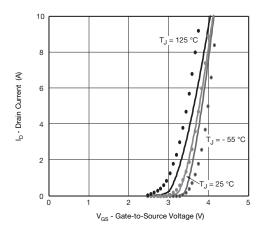
Notes

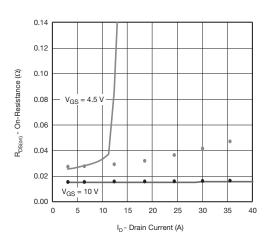
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

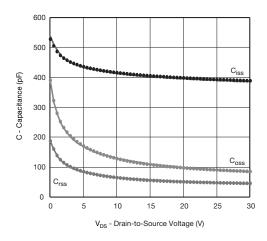
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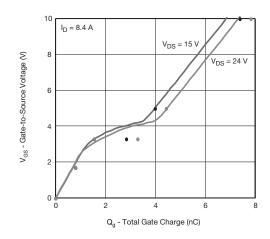
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

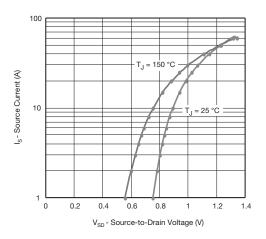












NoteDots and squares represent measured data.



Legal Disclaimer Notice

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