Dual N-Channel 30 V (D-S) MOSFET with Schottky Diode

DESCRIPTION

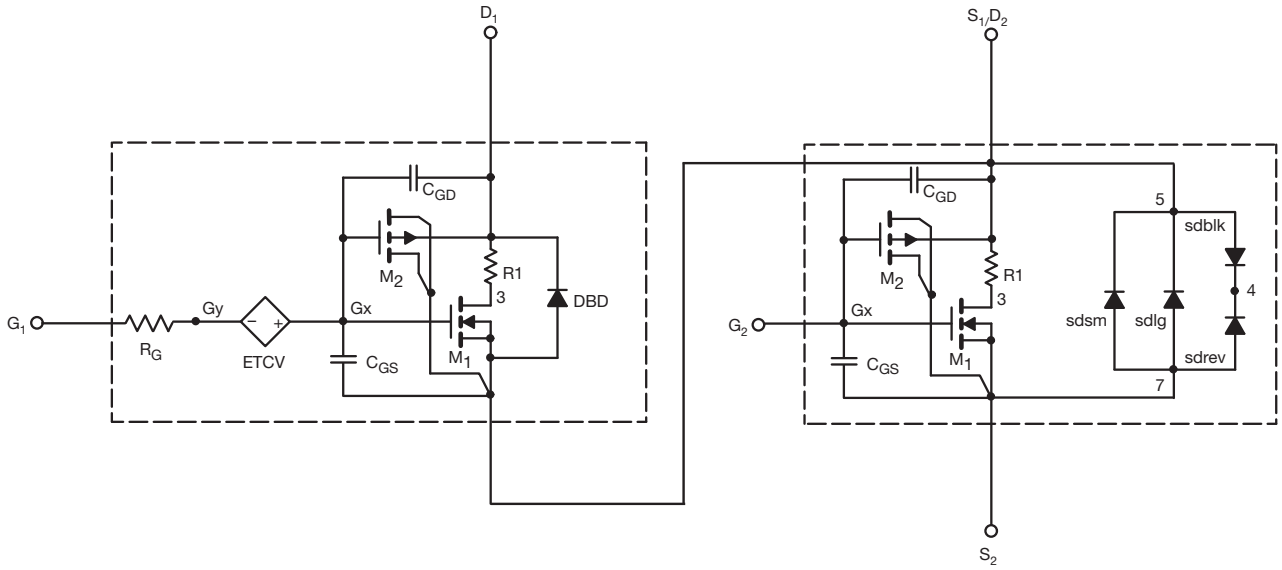
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	Ch-1	1.8	-	V
			Ch-2	1.7	-	
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 8 A	Ch-1	0.0178	0.0175	Ω
		V_{GS} = 10 V, I_D = 8 A	Ch-2	0.0178	0.0175	
		V_{GS} = 4.5 V, I_D = 6 A	Ch-1	0.0208	0.0205	
		V_{GS} = 4.5 V, I_D = 6 A	Ch-2	0.0208	0.0205	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 8 A	Ch-1	29	31	S
		V_{DS} = 15 V, I_D = 8 A	Ch-2	28	31	
Diode Forward Voltage[a]	V_{SD}	I_S = 2 A	Ch-1	0.76	0.75	V
		I_S = 1 A	Ch-2	0.55	0.45	
Dynamic[b]						
Input Capacitance	C_{iss}	Channel-1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	908	900	pF
			Ch-2	872	870	
Output Capacitance	C_{oss}		Ch-1	193	180	
		Channel-2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-2	149	150	
Reverse Transfer Capacitance	C_{rss}		Ch-1	62	60	
			Ch-2	56	56	
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 10 A	Ch-1	13	14	nC
		V_{DS} = 15 V, V_{GS} = 10 V, I_D = 10 A	Ch-2	13	14	
Gate-Source Charge	Q_{gs}	Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A	Ch-1	6.3	6.6	
			Ch-2	6.1	6.6	
		Channel-2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A	Ch-1	2.5	2.5	
			Ch-2	2.5	2.5	
Gate-Drain Charge	Q_{gd}		Ch-1	1.7	1.7	
			Ch-2	1.7	1.7	

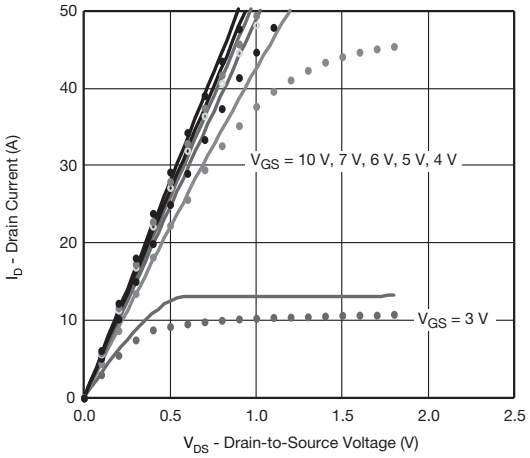
Notes

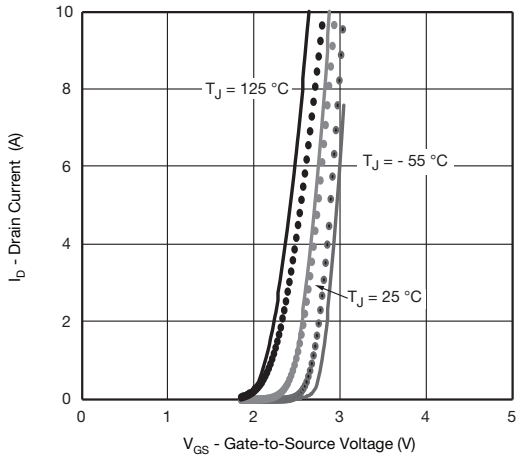
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

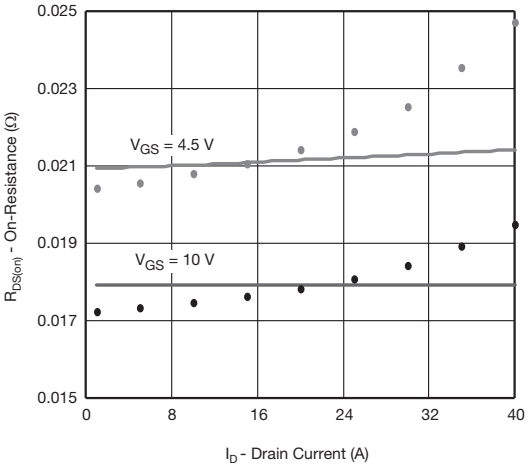
b. Guaranteed by design, not subject to production testing.

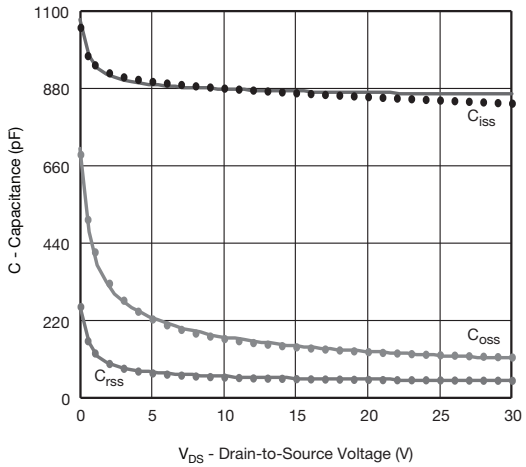
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

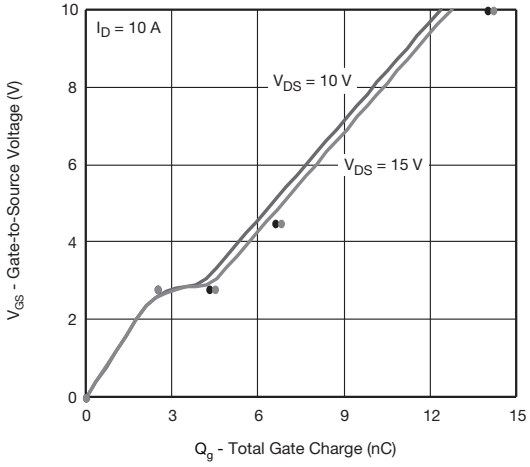
Channel-1 MOSFET

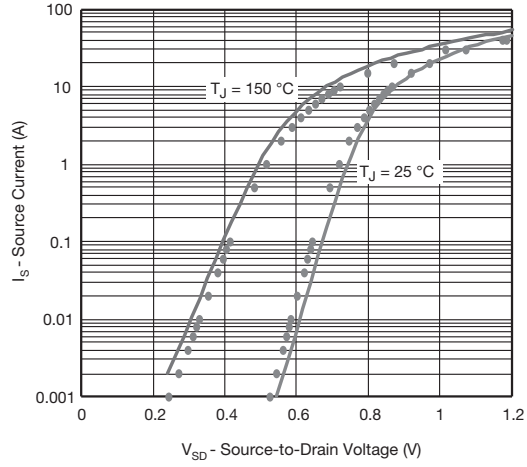










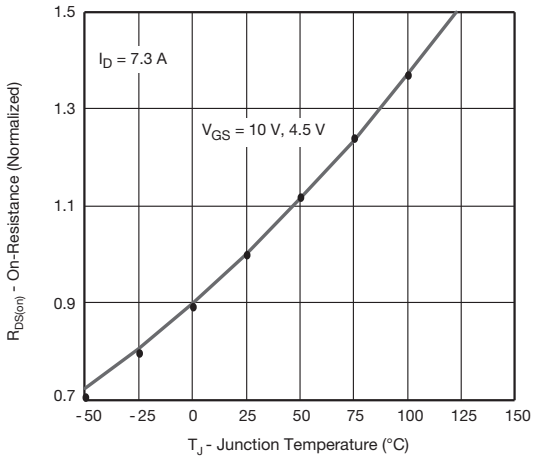


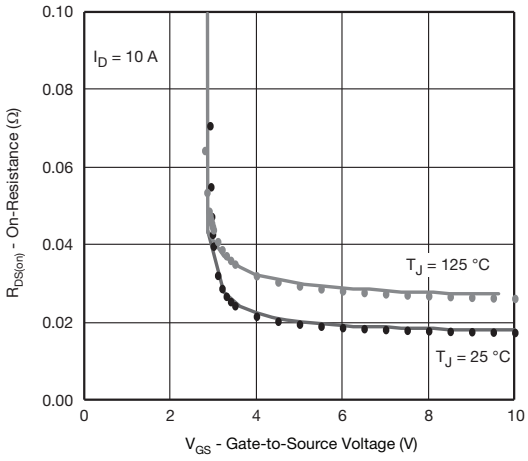
Note

- Dots and squares represent measured data.

COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

Channel-1 MOSFET





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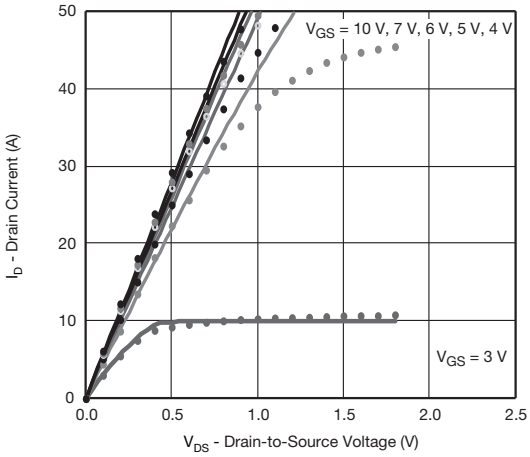
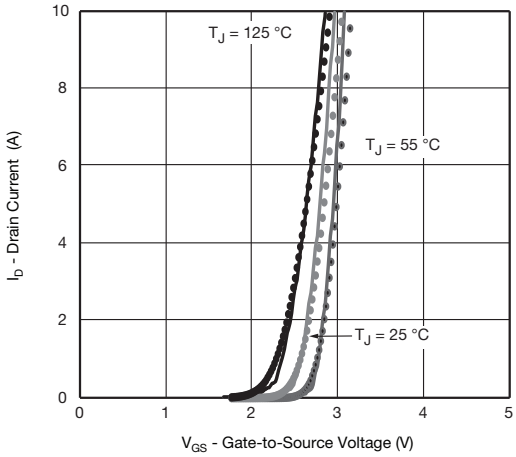
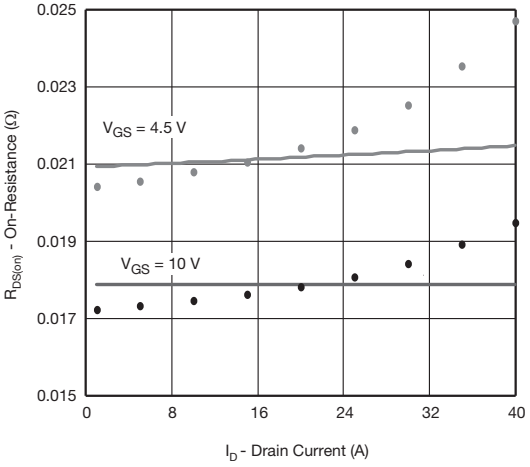
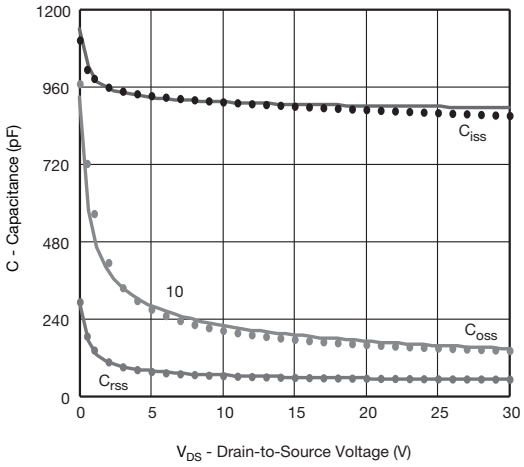
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

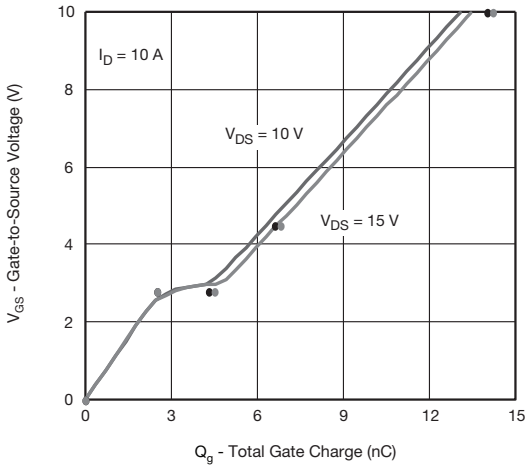
Channel-2 MOSFET

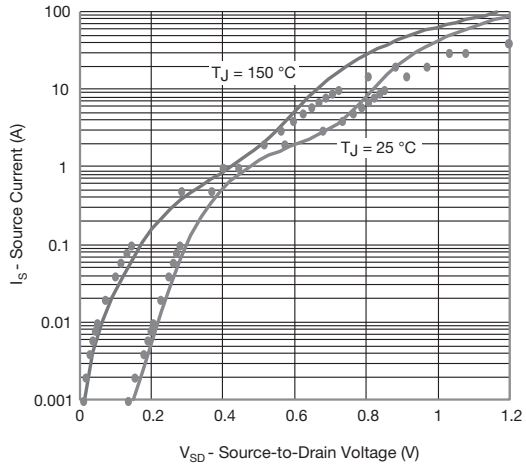












Note

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