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Vishay Siliconix

P-Channel 60 V (D-S) 175 °C MOSFET

DESCRIPTION

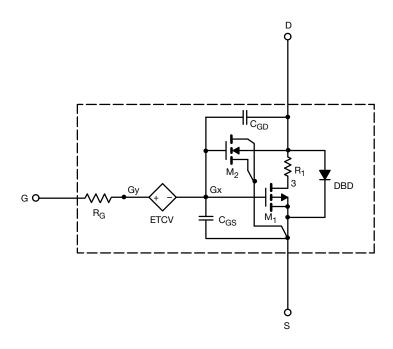
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- · Apply for both Linear and Switching Application
- Accurate over the 55 °C to 125 °C Temperature Range
- · Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPICE Device Model SQ2309ES

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITION	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$	2	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -10 \text{ V}, I_D = -1.25 \text{ A}$	0.267	0.268	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -1 \text{ A}$	0.390	0.370	
Forward Transconductance ^a	g _{fs}	$V_{DS} = -5 \text{ V}, I_D = -1 \text{ A}$	2.8	1.8	S
Diode Forward Voltage	V_{SD}	I _S = - 1.5 A	- 0.85	- 0.85	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = - 25 V, V _{GS} = 0 V, f = 1 MHz	213	211	pF
Output Capacitance	C _{oss}		29	30	
Reverse Transfer Capacitance	C _{rss}		21	21	
Total Gate Charge	Qg		4.4	5.5	
Gate-Source Charge	Q_{gs}	$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -1 \text{ A}$	0.8	0.8	nC
Gate-Drain Charge	Q_{gd}		1.3	1.3	

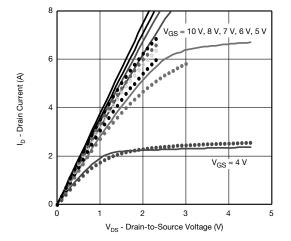
Notes

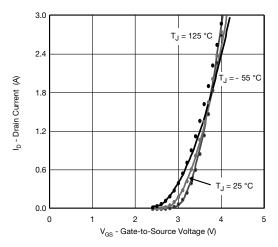
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

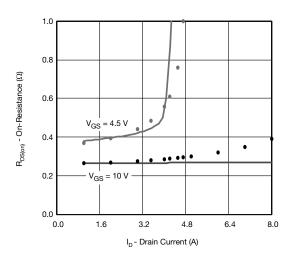
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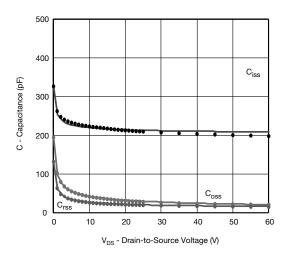
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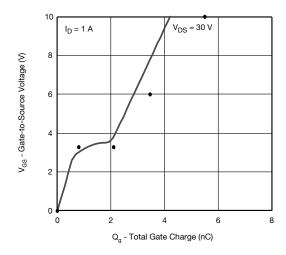
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25~^{\circ}C$, unless otherwise noted)

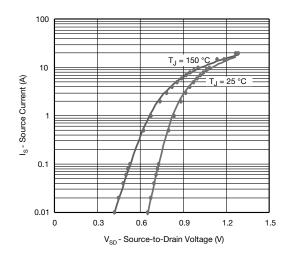












Note

• Dots and squares represent measured data.



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