

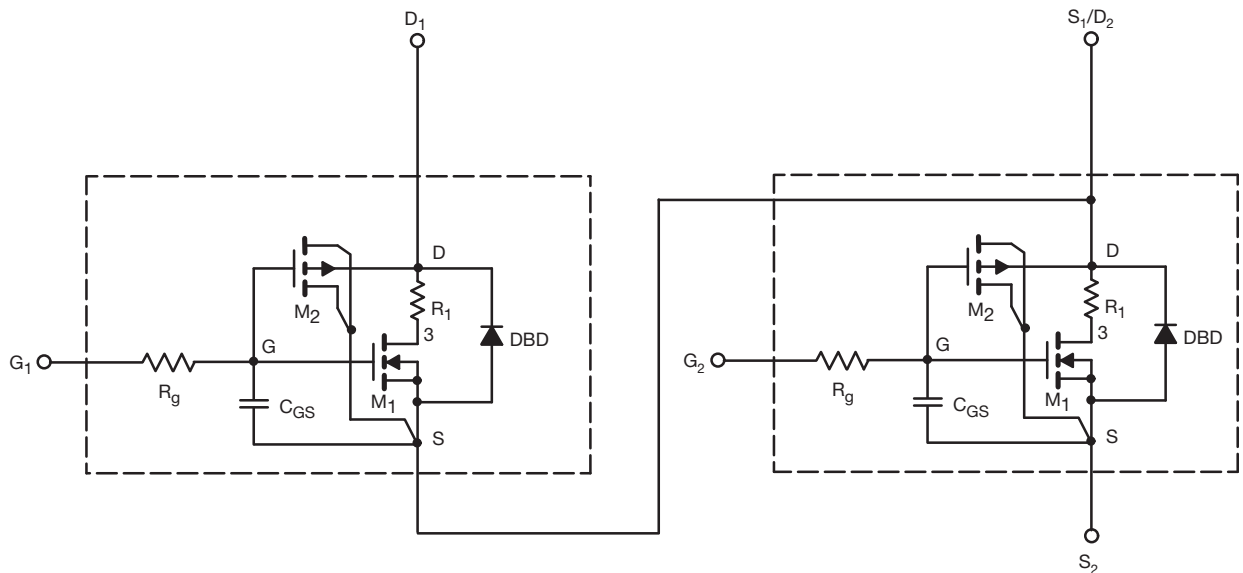
Dual N-Channel 30 V (D-S) MOSFET

DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1.9	-	V	
			Ch-2	1.8	-		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 19.4 A	Ch-1	0.0061	0.0059	Ω	
			Ch-2	0.0032	0.0032		
			V _{GS} = 4.5 V, I _D = 17.2 A	Ch-1	0.0075		0.0075
				Ch-2	0.0039		0.0038
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 19.4 A	Ch-1	64	76	S	
			Ch-2	90	120		
Diode Forward Voltage ^a	V _{SD}	I _S = 10 A	Ch-1	0.80	0.80	V	
			Ch-2	0.80	0.80		
Dynamic^b							
Input Capacitance	C _{iss}	Channel-1 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	1820	1830	pF	
			Ch-2	4850	4900		
Output Capacitance	C _{oss}	Channel-2 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	303	300		
			Ch-2	719	710		
Reverse Transfer Capacitance	C _{rss}	Channel-1 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	123	120		
			Ch-2	289	280		
Total Gate Charge	Q _g	Channel-1 V _{DS} = 15 V, V _{GS} = 10 V, I _D = 19.4 A	Ch-1	28	29	nC	
			Ch-2	73	73		
		Channel-2 V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A	Ch-1	14	13.5		
			Ch-2	35	34		
Gate-Source Charge	Q _{gs}	Channel-1 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 19.4 A	Ch-1	5.8	5.8		
			Ch-2	15	15		
Gate-Drain Charge	Q _{gd}	Channel-2 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A	Ch-1	3.1	3.1		
			Ch-2	7.3	7.3		

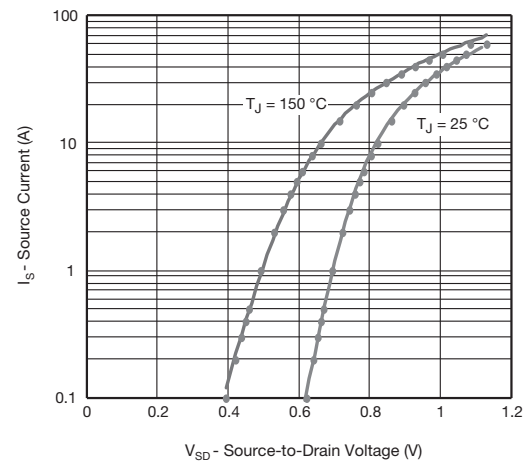
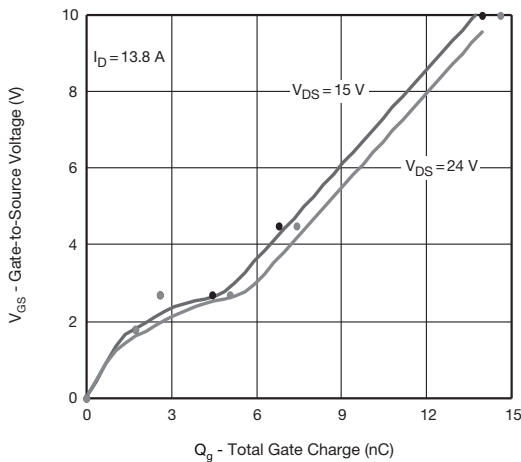
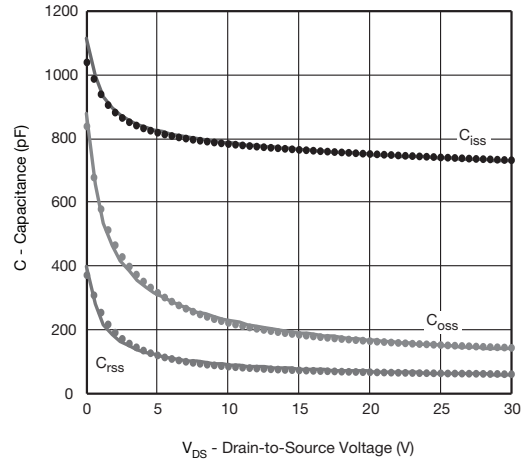
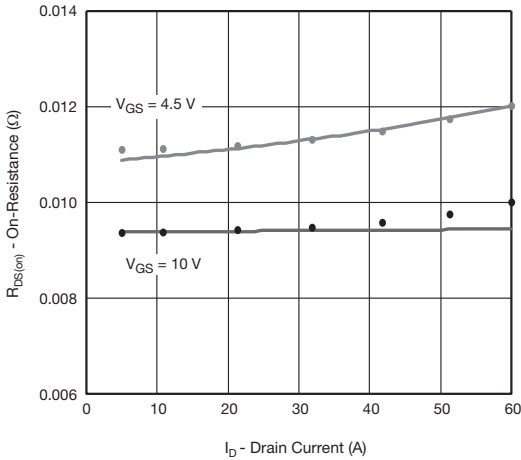
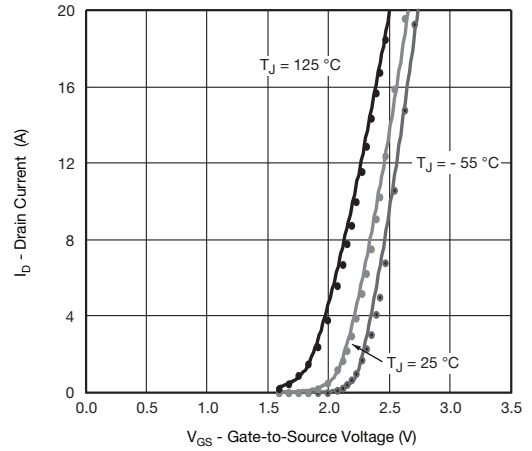
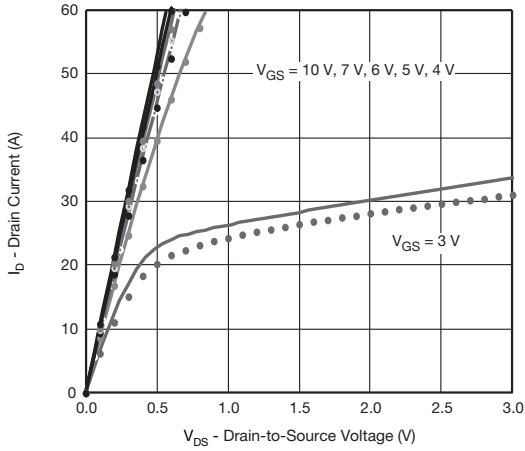
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Channel-1 MOSFET



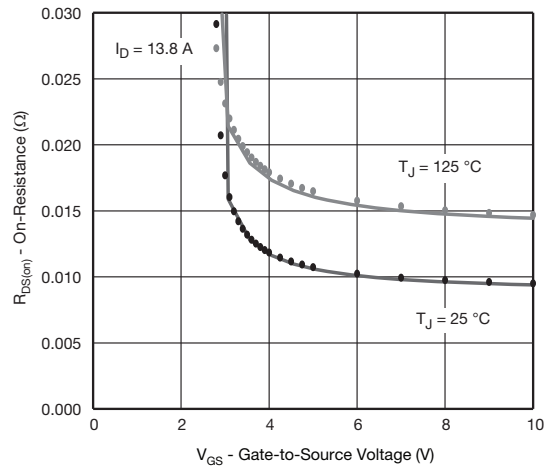
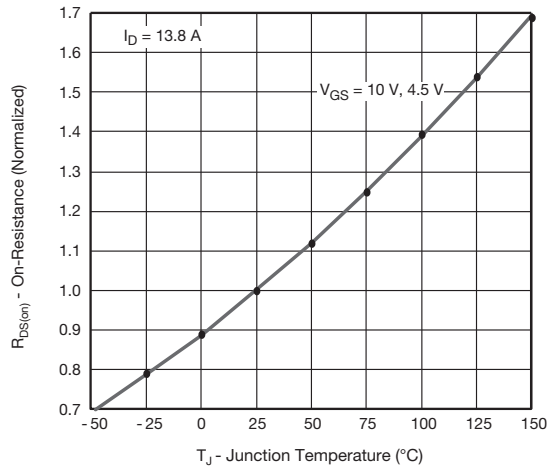
Note

- Dots and squares represent measured data.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Channel-1 MOSFET



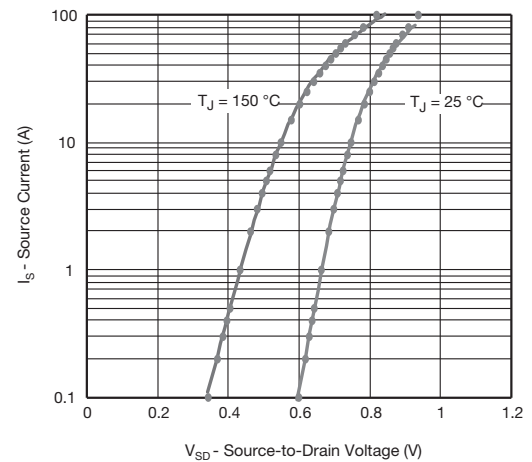
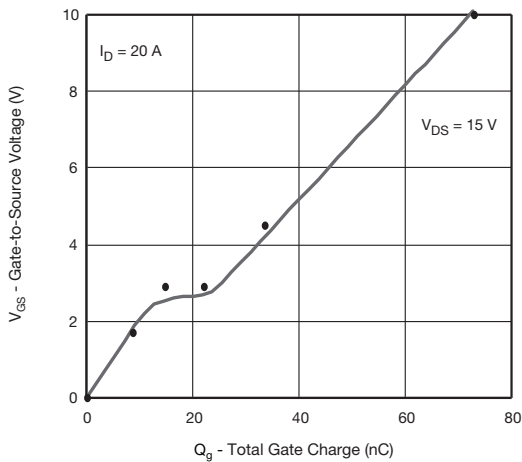
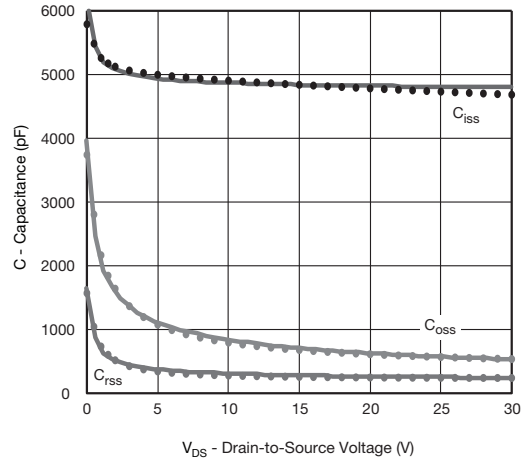
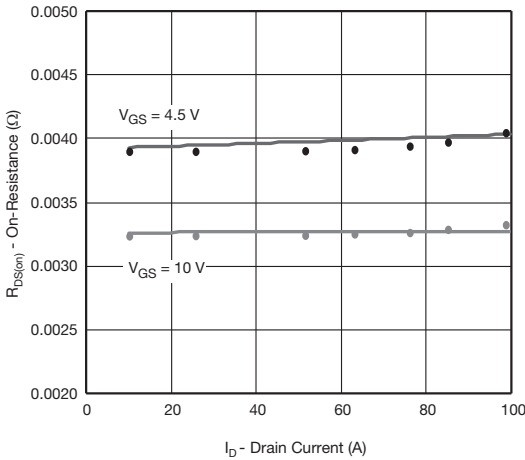
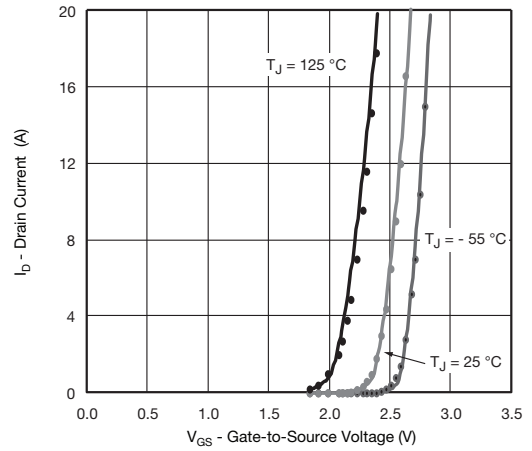
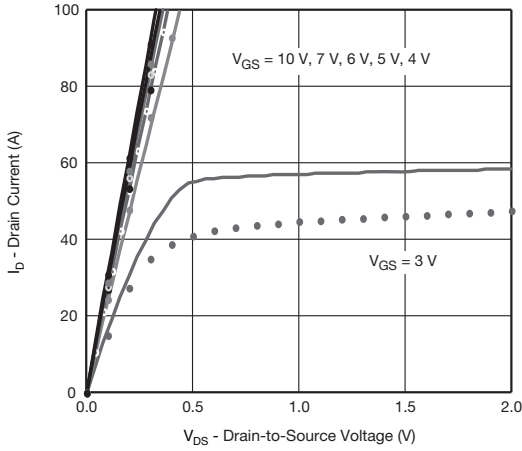
Note

- Dots and squares represent measured data.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Channel-2 MOSFET



Note

- Dots and squares represent measured data.



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