20 mΩ, Slew Rate Controlled Load Switch in WCSP6

DESCRIPTION

SiP32458 and SiP32459 are slew rate controlled integrated high side load switches that operate in the input voltage range from 1.5 V to 5.5 V.

SiP32458 and SiP32459 are of p-channel MOSFET switching element with integrated gate pump that provides 20 mΩ switch on resistance over a wide input voltage range.

These devices have low voltage logic control threshold that can interface with low voltage control I/O directly without extra level shift or driver. A 2.8 MΩ pulldown resistor is integrated at logic control EN pin.

The slow slew rate of SiP32458 and SiP32459 in the range of 3 ms limits the in-rush current and minimized the switching noise.

The SiP32458 features a reverse current blocking capability while the SiP32459 features an integrated output discharge switch.

Both SiP32458 and SiP32459 are available in compact wafer level WCSP package, WCSP6 1 mm x 1.5 mm with 0.5 mm pitch.

FEATURES

- Low input voltage, 1.5 V to 5.5 V
- Low R_{on}, 20 mΩ typical at 5 V
- Slew rate control
- Compatible with 1.2 V logic
- Reverse current blocking when disabled (SiP32458, without output discharge switch)
- Integrated output discharge switch (SiP32459 only)
- Integrated pull down resistor at EN pin
- 6 bumps WCSP package
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE Available

APPLICATIONS

- Battery operated devices
- Smart phones
- GPS and PMP
- Computer
- Medical and healthcare equipment
- Industrial and instrument
- Cellular phones and portable media players
- Game console

TYPICAL APPLICATION CIRCUIT

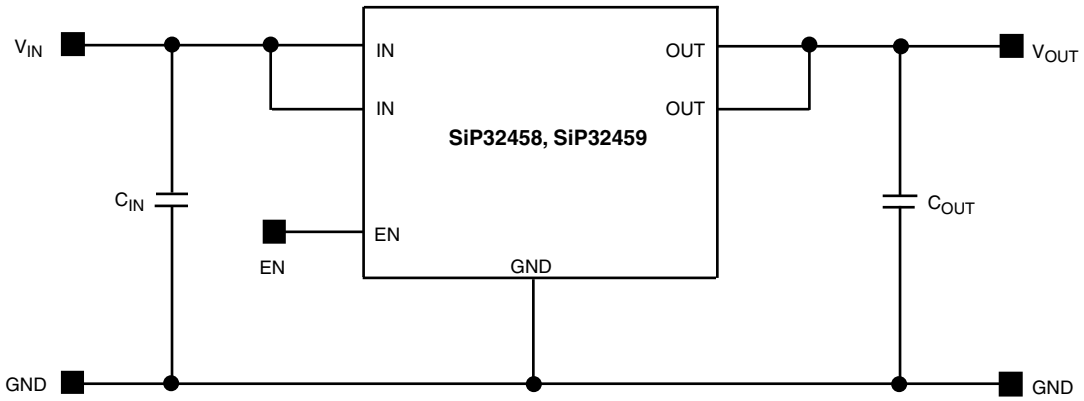


Fig. 1 - SiP32458 and SiP32459 Typical Application Circuit

ORDERING INFORMATION			
TEMPERATURE RANGE	**PACKAGE**	**MARKING**	**PART NUMBER**
-40 °C to +85 °C	WCSP: 6 bumps (2 x 3, 0.5 mm pitch, 250 µm bump height, 1.5 mm x 1 mm die size)	AA	SiP32458DB-T2-GE1
		AB	SiP32459DB-T2-GE1

Note

- -GE1 denotes halogen-free and RoHS-compliant

ABSOLUTE MAXIMUM RATINGS

PARAMETER	LIMIT	UNIT
Supply input voltage (V_{IN})	-0.3 to 6	V
Enable input voltage (V_{EN})	-0.3 to 6	
Output voltage (V_{OUT})	-0.3 to 6	
Maximum continuous switch current ($I_{max.}$)	3	A
Maximum pulsed current (I_{DM}) V_{IN} (pulsed at 1 ms, 10 % duty cycle)	6	
ESD rating (HBM)	4000	V
Junction temperature (T_J)	-40 to +150	°C
Thermal resistance (θ_{JA}) [a]	110	°C/W
Power dissipation (P_D) [a]	500	mW

Notes

a. Device mounted with all bumps soldered to PC board

b. Derate 9.1 mW/°C above T_A = 70 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

PARAMETER	LIMIT	UNIT
Input voltage range (V_{IN})	1.5 to 5.5	V
Operating junction temperature range	-40 to +125	°C

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = 1.5 V to 5.5 V, T_A = -40 °C to +85 °C (typical values are at V_{IN} = 4.5 V, T_A = 25 °C)	LIMITS MIN. [a]	LIMITS TYP. [b]	LIMITS MAX. [a]	UNIT
Operating voltage [c]	V_{IN}		1.5	-	5.5	V
Quiescent current	I_Q	V_{EN} = V_{IN}, OUT = open	-	4.2	9.5	µA
Off supply current	$I_{Q(off)}$	SiP32458, EN = GND, OUT = open	-	-	1	
		SiP32459, EN = GND, OUT = open	-	-	10	
Off switch current	$I_{DS(off)}$	EN = GND, OUT = 0 V	-	-	10	
Reverse blocking current	I_{RB}	V_{OUT} = 2.5 V, V_{IN} = 0.75 V, V_{EN} = 0 V (SiP32458 only)	-	-	10	
On-resistance	$R_{DS(on)}$	V_{IN} = 1.5 V, I_L = 500 mA, T_A = 25 °C	-	30	36	mΩ
		V_{IN} = 1.8 V, I_L = 500 mA, T_A = 25 °C	-	26	32	
		V_{IN} = 3.3 V, I_L = 500 mA, T_A = 25 °C	-	20	26	
		V_{IN} = 5 V, I_L = 1 A, T_A = 25 °C	-	20	26	
On-resistance temp. coefficient	TC_{RDS}		-	2820	-	ppm/°C
Output pulldown resistance	R_{PD}	V_{IN} = 3.3 V, I_{OUT} = 5 mA, V_{EN} = 0 V (SiP32459 only)	-	70	-	W
EN input low voltage [c]	V_{IL}	V_{IN} = 1.5 V	-	-	0.4	V
EN input high voltage [c]	V_{IH}	V_{IN} = 5.5 V	1	-	-	
EN input leakage	I_{EN}	V_{IN} = 5.5 V, V_{EN} = 0 V	-	-	1	µA
		V_{IN} = 5.5 V, V_{EN} = 1.2 V	-	0.44	1	
EN pulldown resistor	R_{EN}	V_{IN} = 5.5 V, V_{EN} = 1.2 V	-	2.8	-	MΩ
Output turn-on delay time	$t_{d(on)}$	V_{IN} = 4.5 V, R_{LOAD} = 5 Ω, C_L = 100 µF, T_A = 25 °C	-	0.5	-	ms
Output turn-on rise time	t_r		-	3	-	
Output turn-off delay time	$t_{d(off)}$		-	18	-	µs

Notes

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum

b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing

c. For V_{IN} outside this range consult typical EN threshold curve

PIN CONFIGURATION

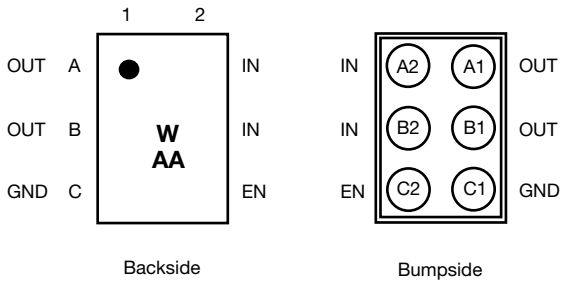


Fig. 2 - WCSP 2 x 3 Package

PIN DESCRIPTION		
PIN NUMBER	**NAME**	**FUNCTION**
A1, B1	OUT	These are the output pins of the switch
C1	GND	Ground connection
A2, B2	IN	These are input pins of the switch
C2	EN	Enable input

BLOCK DIAGRAM

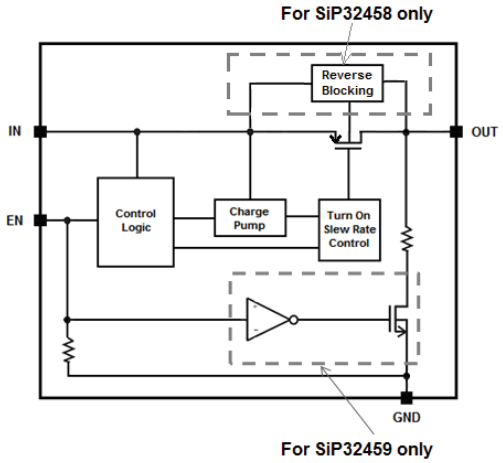


Fig. 3 - Functional Block Diagram

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

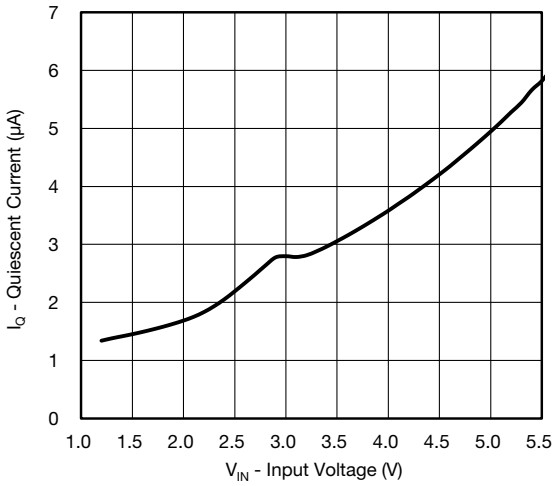


Fig. 4 - Quiescent Current vs. Input Voltage

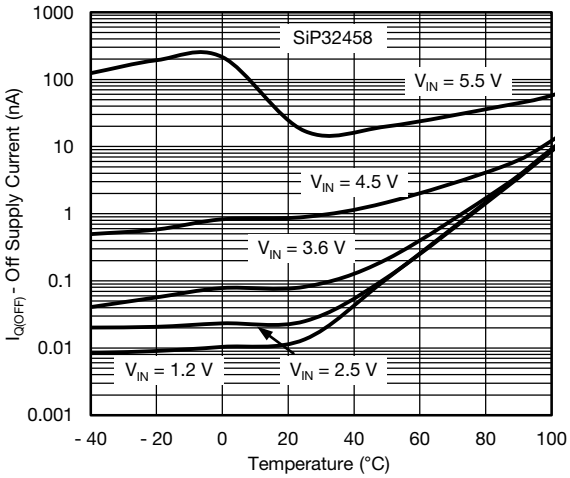


Fig. 7 - Off Supply Current vs. Temperature

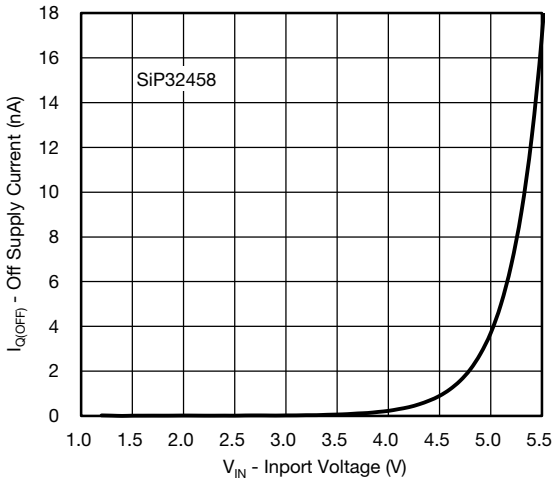


Fig. 5 - Off Supply Current vs. Input Voltage

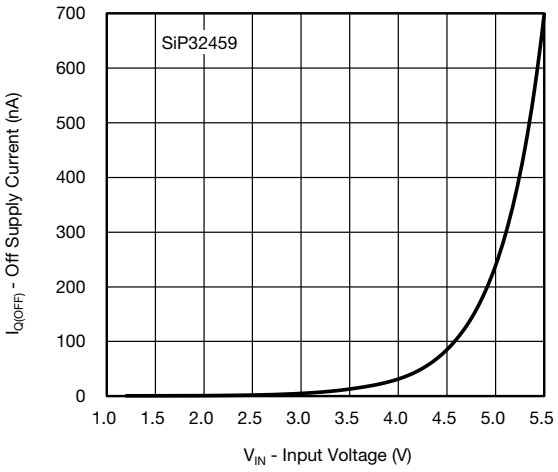


Fig. 8 - Off Supply Current vs. Input Voltage

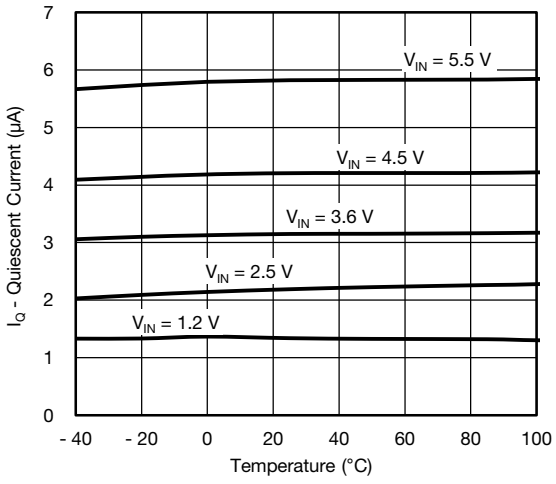


Fig. 6 - Quiescent Current vs. Temperature

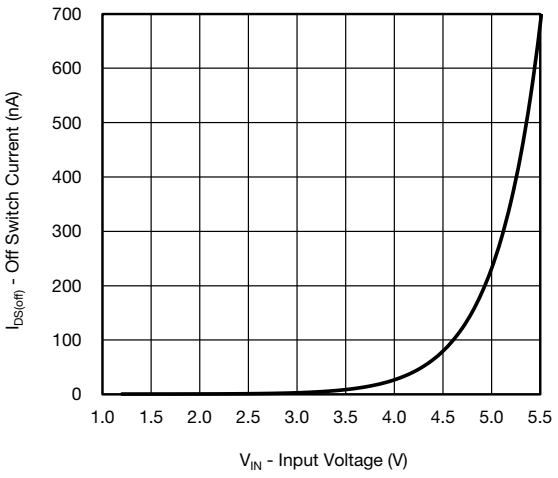


Fig. 9 - Off Switch Current vs. Input Voltage

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

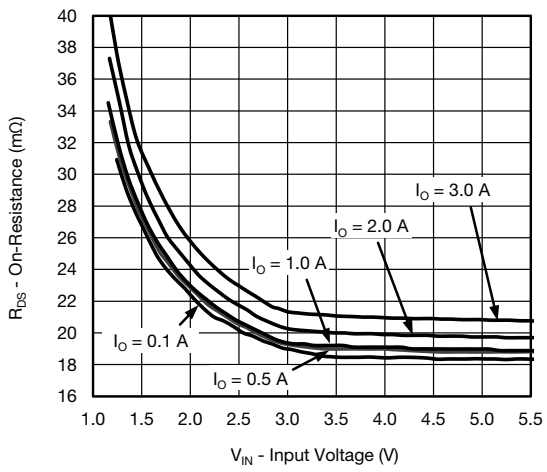


Fig. 10 - $R_{DS(on)}$ vs. Input Voltage

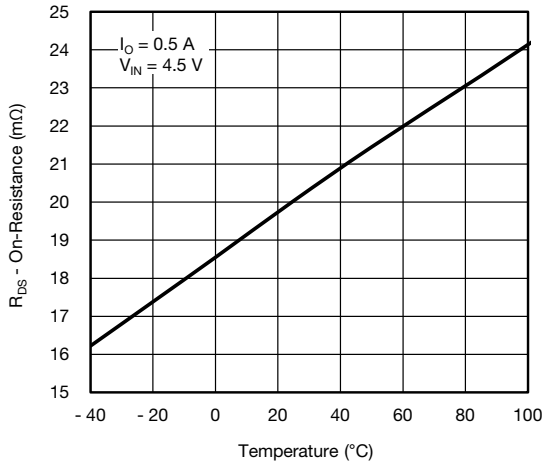


Fig. 13 - $R_{DS(on)}$ vs. Temperature

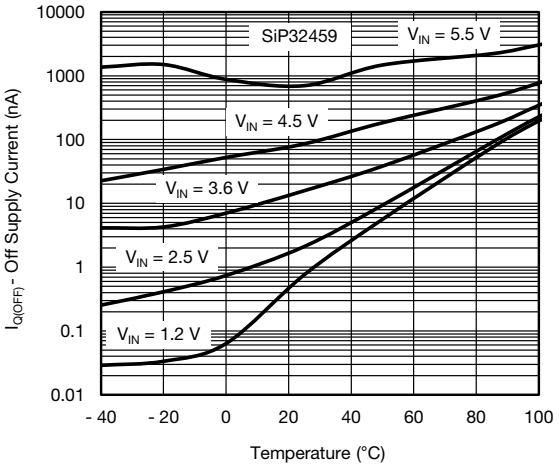


Fig. 11 - Off Supply Current vs. Temperature

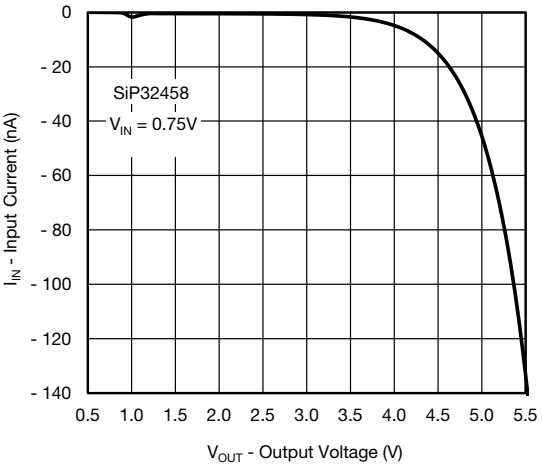


Fig. 14 - Reverse Blocking Current vs. Output Voltage

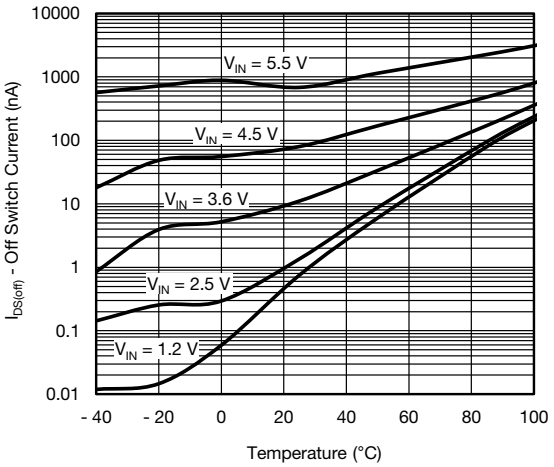


Fig. 12 - Off Switch Current vs. Temperature

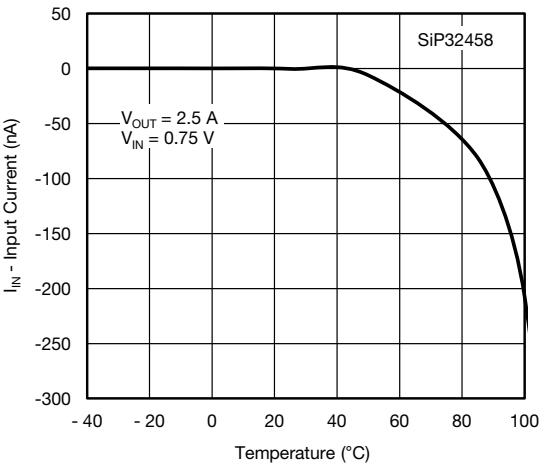


Fig. 15 - Reverse Blocking Current vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

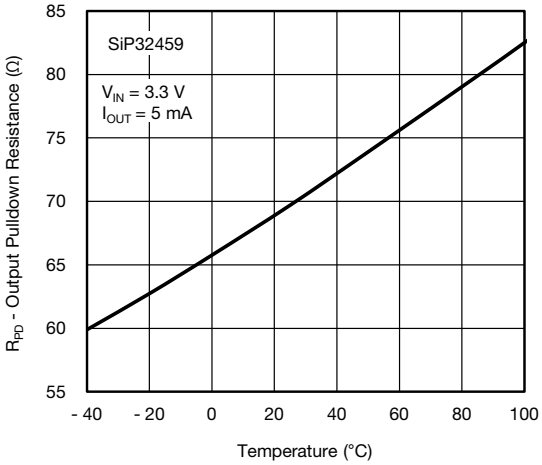


Fig. 16 - Output Pulldown Resistance vs. Temperature

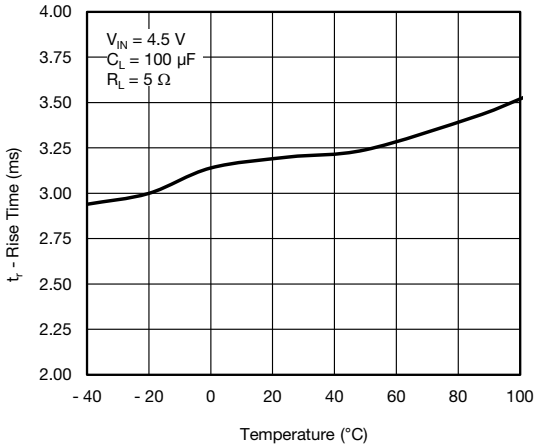


Fig. 19 - Rise Time vs. Temperature

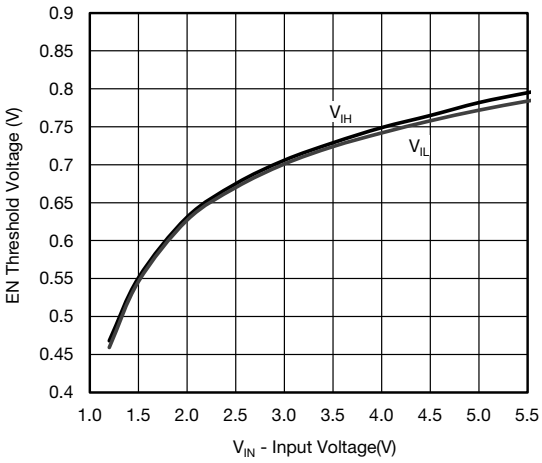


Fig. 17 - EN Threshold Voltage vs. Input Voltage

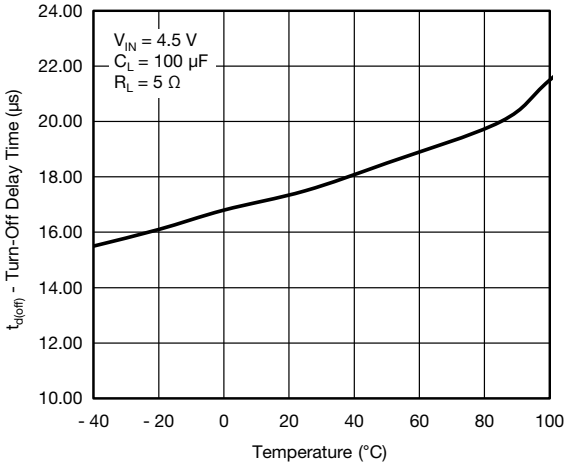


Fig. 20 - Turn-Off Delay Time vs. Temperature

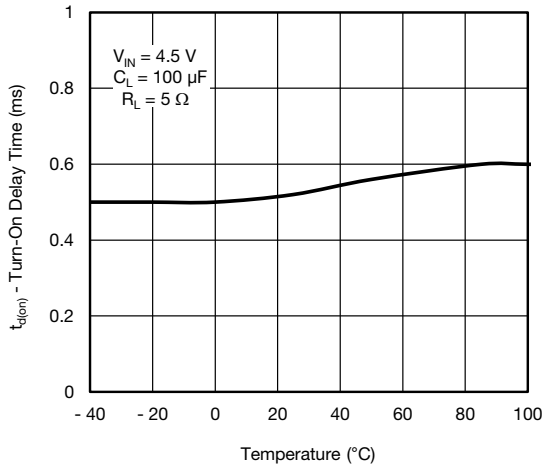


Fig. 18 - Turn-On Delay Time vs. Temperature

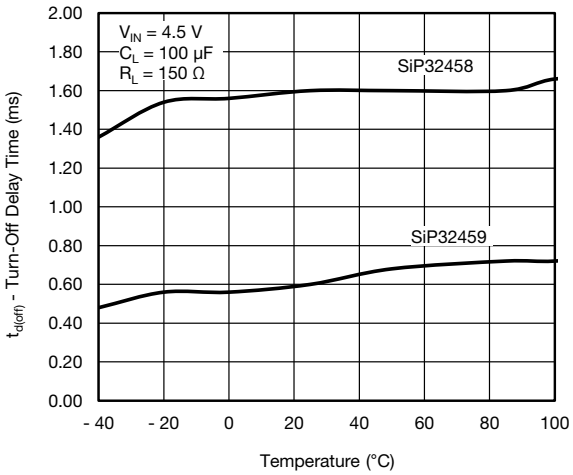


Fig. 21 - Turn-Off Delay Time vs. Temperature

TYPICAL WAVEFORMS

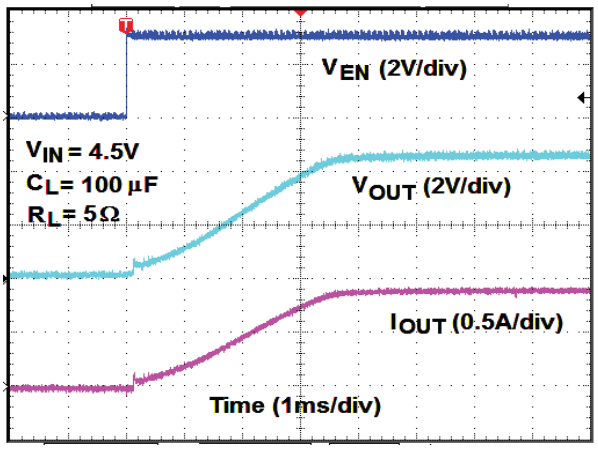


Fig. 22 - Turn-On Time

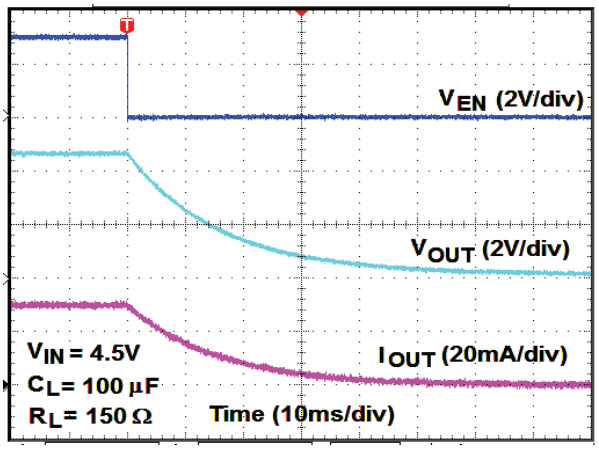


Fig. 25 - Turn-Off Time, SiP32458

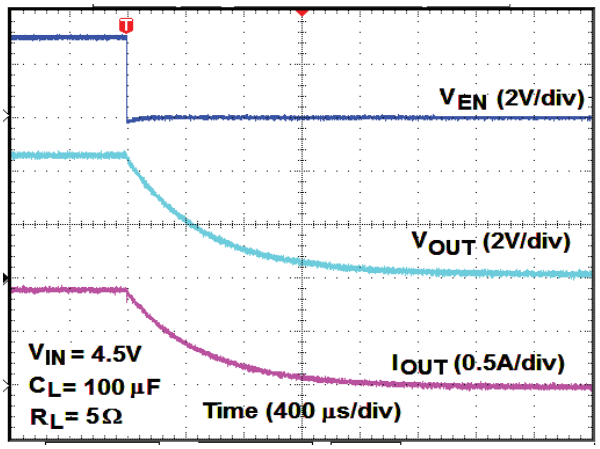


Fig. 23 - Turn-Off Time

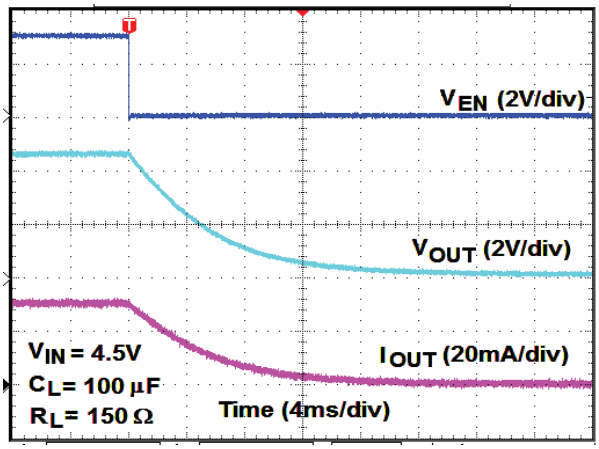


Fig. 26 - Turn-Off Time, SiP32459

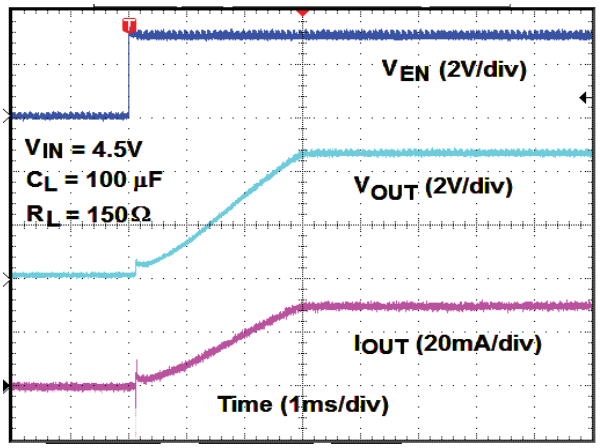


Fig. 24 - Turn-On Time

DETAILED DESCRIPTION

SiP32458 and SiP32459 are p-channel power MOSFET designed as high side load switches. They incorporate a negative charge pump at the gate to keep the gate to source voltage high when turned on therefore keep the on resistance low at lower input voltage range. SiP32458 and SiP32459 are designed with slow slew rate to minimize the inrush current during turn on. The SiP32458 has a reverse blocking circuit to prevent the current from going back to the input in case the output voltage is higher than the input voltage. The SiP32459 has an output pulldown resistor to discharge the output capacitance when the device is off.

APPLICATION INFORMATION

Input Capacitor

While a bypass capacitor on the input is not required, a 4.7 µF or larger capacitor for C_{IN} is recommended in almost all applications. The bypass capacitor should be placed as physically close as possible to the input pin to be effective in minimizing transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 0.1 µF capacitor across V_{OUT} and GND is recommended to insure proper slew operation. There is inrush current through the output MOSFET and the magnitude of the inrush current depends on the output capacitor, the bigger the C_{OUT} the higher the inrush current. There are no ESR or capacitor type requirement.

Enable

The EN pin is compatible with CMOS logic voltage levels. It requires at least 0.4 V or below to fully shut down the device and 1 V or above to fully turn on the device. There is a 2.8 MΩ resistor connected between EN pin and GND pin.

Protection Against Reverse Voltage Condition

The SiP32458 contains the reverse blocking circuit to keep the output current from flowing back to the input in case the output voltage is higher than the input voltage.

Thermal Considerations

These devices are designed to maintain a constant output load current. Due to physical limitations of the layout and assembly of the device the maximum switch current is 3 A as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation (and a thermal resistance of 110 °C/W) the device should be connected to a heat sink on the printed circuit board.

The maximum power dissipation in any application is dependent on the maximum junction temperature, T_J (max.) = 125 °C, the junction-to-ambient thermal resistance, θ_{J-A} = 110 °C/W, and the ambient temperature, T_A, which may be formulaically expressed as:

$$P\ (max.) = \frac{T_{J(max.)} - T_A}{\theta_{JA}} = \frac{125 - T_A}{280}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 500 mW.

So long as the load current is below the 3 A limit, the maximum continuous switch current becomes a function two things: the package power dissipation and the $R_{DS(on)}$ at the ambient temperature.

As an example let us calculate the worst case maximum load current at T_A = 70 °C. The worst case $R_{DS(on)}$ at 25 °C is 36 mΩ at V_{IN} = 1.5 V. The $R_{DS(on)}$ at 70 °C can be extrapolated from this data using the following formula:

$R_{DS(on)}$ (at 70 °C) = $R_{DS(on)}$ (at 25 °C) x (1 + T_C x ΔT)

Where T_C is 2820 ppm/°C. Continuing with the calculation we have

$R_{DS(on)}$ (at 70 °C) = 36 mΩ x (1 + 0.00282 x (70 °C - 25 °C)) = 40.5 mΩ

The maximum current limit is then determined by

$$I_{LOAD(max.)} < \sqrt{\frac{P\ (max.)}{R_{DS(on)}}}$$

which in this case is 3.5 A. Under the stated input voltage condition, if the 3.5 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

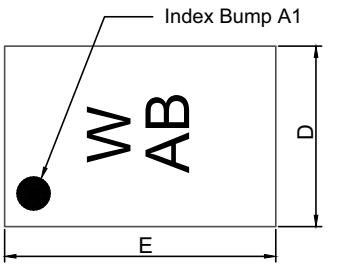
To avoid possible permanent damage to the device and keep a reasonable design margin, it is recommended to operate the device maximum up to 3 A only as listed in the Absolute Maximum Ratings table.

PRODUCT SUMMARY		
Part number	SiP32458	SiP32459
Description	1.5 V to 5.5 V, 20 mΩ, bidirectional off isolation	1.5 V to 5.5 V, 20 mΩ, output discharge
Configuration	Single	Single
Slew rate time (µs)	3000	3000
On delay time (µs)	500	500
Input voltage min. (V)	1.5	1.5
Input voltage max. (V)	5.5	5.5
On-resistance at input voltage min. (mΩ)	30	30
On-resistance at input voltage max. (mΩ)	20	20
Quiescent current at input voltage min. (µA)	1.5	1.5
Quiescent current at input voltage max. (µA)	5.8	5.8
Output discharge (yes / no)	No	Yes
Reverse blocking (yes / no)	Yes	No
Continuous current (A)	3	3
Package type	WCSP6	WCSP6
Package size (W, L, H) (mm)	1.0 x 1.5 x 0.5	1.0 x 1.5 x 0.5
Status code	2	2
Product type	Slew rate	Slew rate
Applications	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable

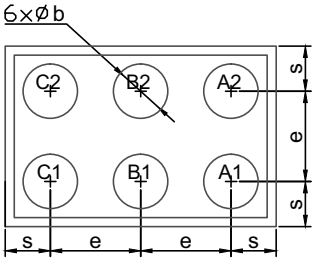
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63999.

WCSP6: 6 Bumps

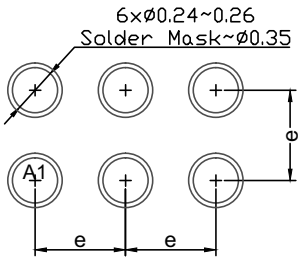
(2 x 3, 0.5 mm pitch, 250 µm bump height, 1 mm x 1.5 mm die size)



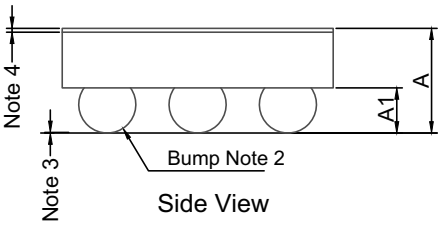
Top View



Bottom View



RECOMMENDED
LAND PATTERN



Side View

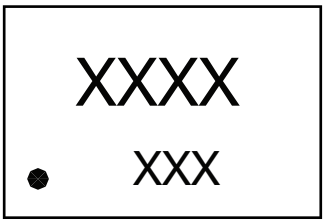
DIMENSION	MILLIMETERS (5)			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.540	0.572	0.620	0.0212	0.0225	0.0244
A1	0.214	0.250	0.286	0.0084	0.0098	0.0113
b	0.279	0.310	0.372	0.0109	0.0122	0.0146
e		0.500			0.0197	
s	0.230	0.250	0.270	0.0090	0.0098	0.0106
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
E	1.420	1.460	1.500	0.0559	0.0575	0.0591

Notes (unless otherwise specified)

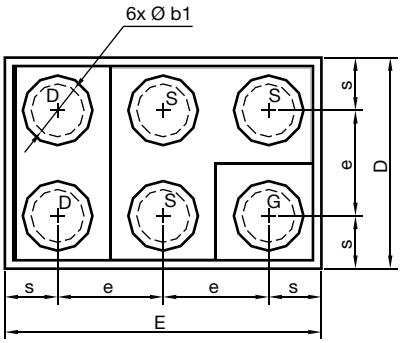
(1) Laser mark on the silicon die back coated with an epoxy film.
(2) Bumps are SAC396.
(3) 0.050 max. co-planarity.
(4) Laminate tape thickness is 0.022 mm.
(5) Use millimeters as the primary measurement.

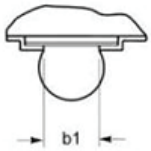
ECN: S13-1424-Rev. B, 01-Jul-13
DWG: 6011

MICRO FOOT®: 6-Bump
(1.5 mm x 1 mm, 0.5 mm Pitch, 0.250 mm Bump Height)

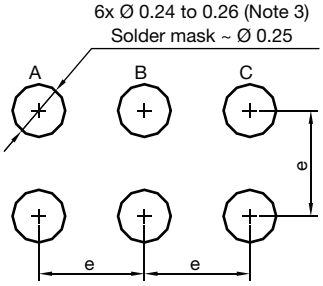


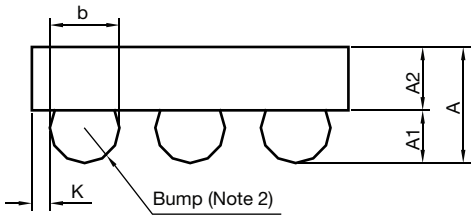
Mark on Backside of Die





NOTE 5





Recommended Land Pattern

Notes

(unless otherwise specified)

1. Six (6) solder bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ti/Ni/Ag layer.
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back.
5. “b1” is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
6. • is the location of pin 1

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.510	0.575	0.590	0.0201	0.0226	0.0232
A_1	0.220	0.250	0.280	0.0087	0.0098	0.0110
A_2	0.290	0.300	0.310	0.0114	0.0118	0.0122
b	0.297	0.330	0.363	0.0116	0.0129	0.0143
b1		0.250			0.0098	
e		0.500			0.0197	
s	0.210	0.230	0.250	0.0082	0.0090	0.0098
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
E	1.420	1.460	1.500	0.0559	0.0575	0.0591
K	0.028	0.065	0.102	0.0011	0.0025	0.0040

Note

- Use millimeters as the primary measurement.

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DWG: 6035

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