

### N-Channel 30-V (D-S) MOSFET

#### CHARACTERISTICS

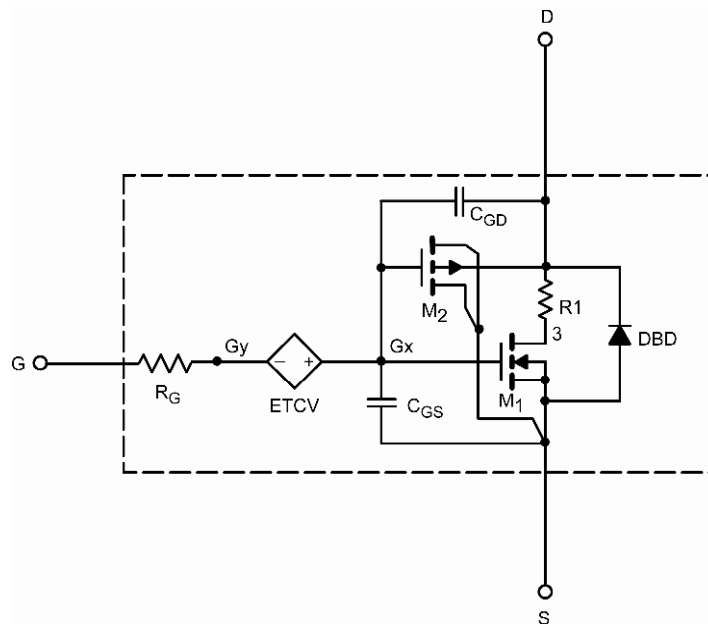
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the N-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



| SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED) |              |  |                |               |          |
|---|--------------|--|----------------|---------------|----------|
| Parameter   | Symbol       | Test Condition   | Simulated Data | Measured Data | Unit     |
| <b>Static</b>   |              |  |                |               |          |
| Gate Threshold Voltage  | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$                  | 1.7            |               | V        |
| Drain-Source On-State Resistance <sup>a</sup>                             | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 20\text{ A}$                        | 0.0050         | 0.0048        | $\Omega$ |
|   |              | $V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$                       | 0.0068         | 0.0065        |          |
| Forward Transconductance <sup>a</sup>                                     | $g_{fs}$     | $V_{DS} = 10\text{ V}, I_D = 20\text{ A}$                        | 69             | 50            | S        |
| Body Diode Voltage  | $V_{SD}$     | $I_S = 3\text{ A}$   | 0.74           | 0.75          | V        |
| <b>Dynamic<sup>b</sup></b>  |              |  |                |               |          |
| Input Capacitance   | $C_{iss}$    | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$    | 1610           | 1600          | pF       |
| Output Capacitance  | $C_{oss}$    |  | 341            | 335           |          |
| Reverse Transfer Capacitance  | $C_{rss}$    |  | 121            | 115           |          |
| Total Gate Charge   | $Q_g$        | $V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$  | 26             | 30            | nC       |
|   |              |  | 13.2           | 13.7          |          |
| Gate-Source Charge  | $Q_{gs}$     | $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$ | 4.3            | 4.3           |          |
| Gate-Drain Charge   | $Q_{gd}$     |  | 4.3            | 4.3           |          |

**Notes**

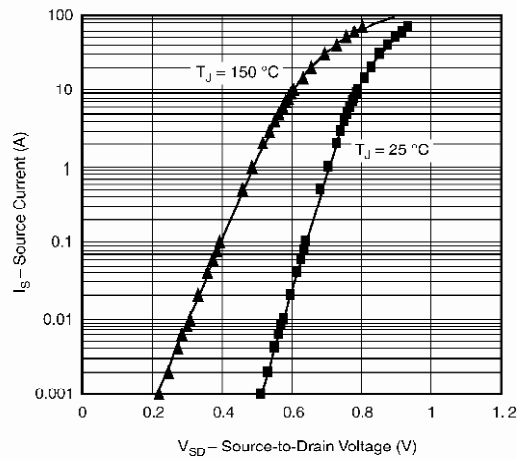
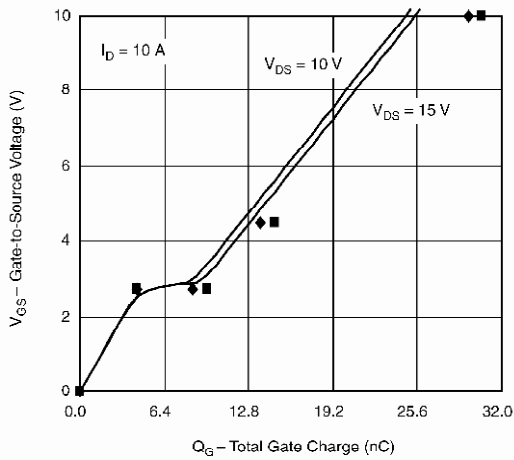
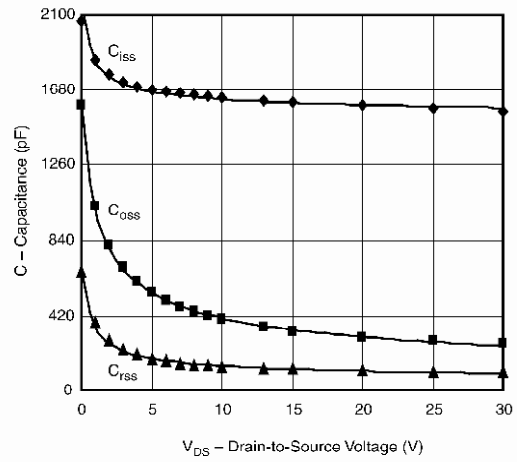
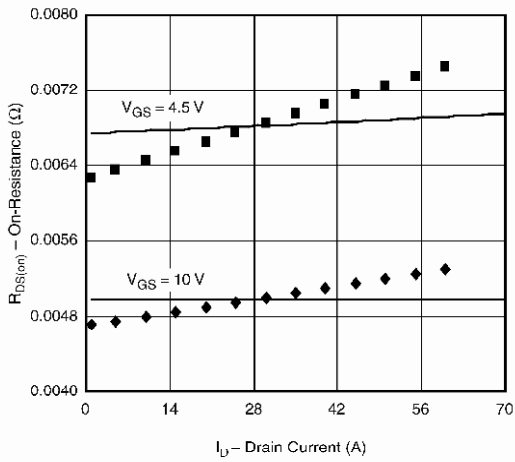
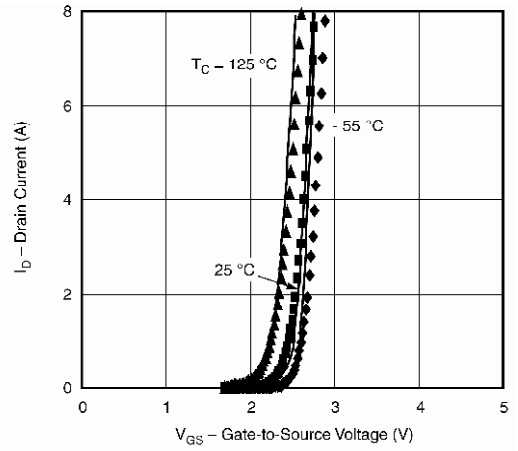
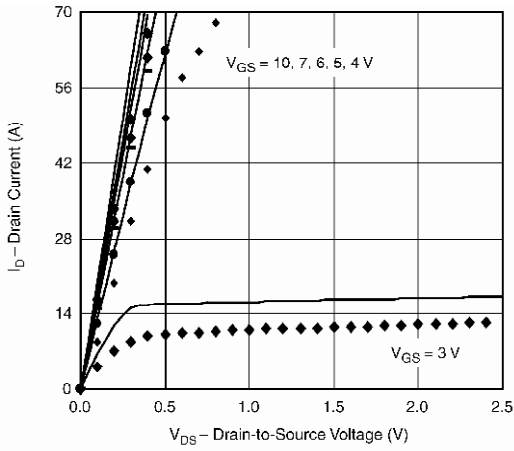
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.



# SPICE Device Model Si7784DP

## Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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