N-Channel Dual Asymmetric 40 V (D-S) 175 °C MOSFET

DESCRIPTION

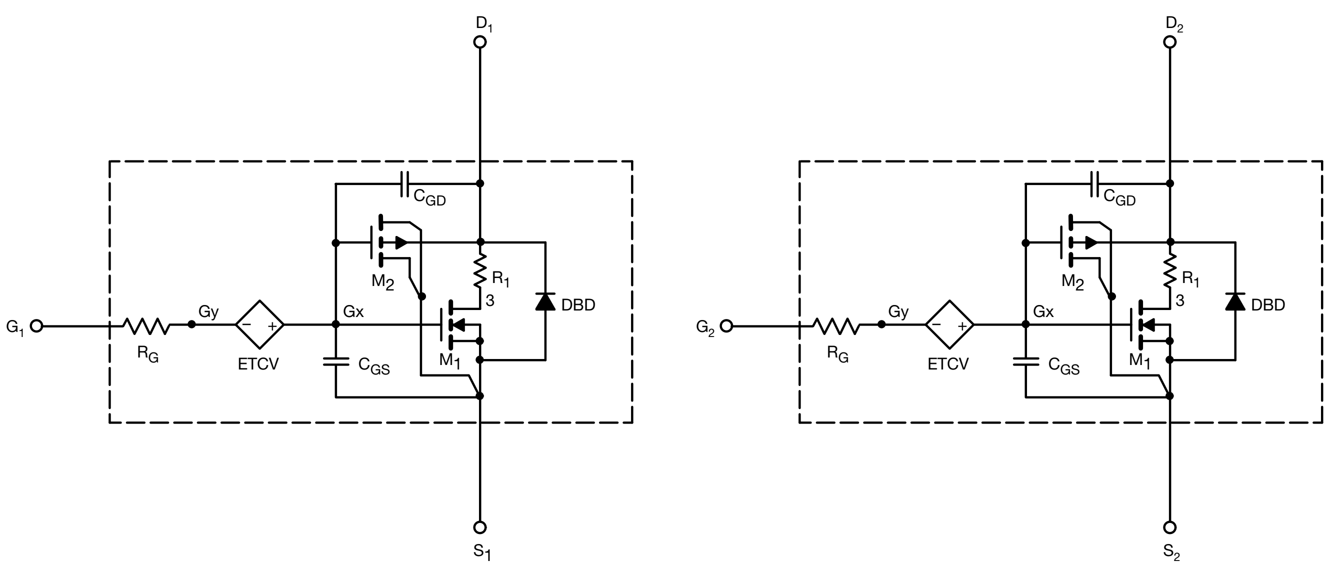
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	Ch-1	1.9	1.8	V
			Ch-2	2	1.8	
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 7.8 A	Ch-1	0.017	0.018	Ω
		V_{GS} = 10 V, I_D = 10.1 A	Ch-2	0.008	0.009	
		V_{GS} = 4.5 V, I_D = 7.1 A	Ch-1	0.021	0.022	
		V_{GS} = 4.5 V, I_D = 9.3 A	Ch-2	0.010	0.011	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 7.8 A	Ch-1	38	46	S
		V_{DS} = 15 V, I_D = 10.1 A	Ch-2	62	73	
Diode Forward Voltage[a]	V_{SD}	I_S = 5.2 A	Ch-1	0.8	0.8	V
		I_S = 6.8 A	Ch-2	0.8	0.8	
Dynamic[b]						
Input Capacitance	C_{iss}	N-Channel V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	647	647	pF
			Ch-2	1170	1161	
Output Capacitance	C_{oss}		Ch-1	107	105	
			Ch-2	181	178	
Reverse Transfer Capacitance	C_{rss}		Ch-1	42	42	
			Ch-2	68	68	
Total Gate Charge	Q_g	Channel 1 V_{DS} = 20 V, V_{GS} = 10 V, I_D = 16 A Channel 2 V_{DS} = 20 V, V_{GS} = 10 V, I_D = 6 A	Ch-1	11	13.1	nC
			Ch-2	19	22.5	
Gate-Source Charge	Q_{gs}		Ch-1	2.12	2.12	
			Ch-2	3.35	3.35	
Gate-Drain Charge	Q_{gd}		Ch-1	1.84	1.84	
			Ch-2	3.14	3.14	

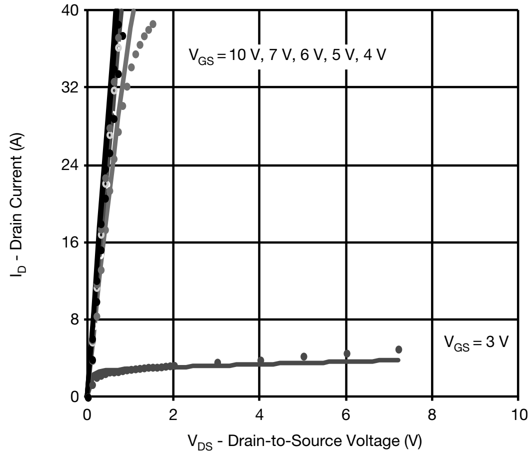
Notes

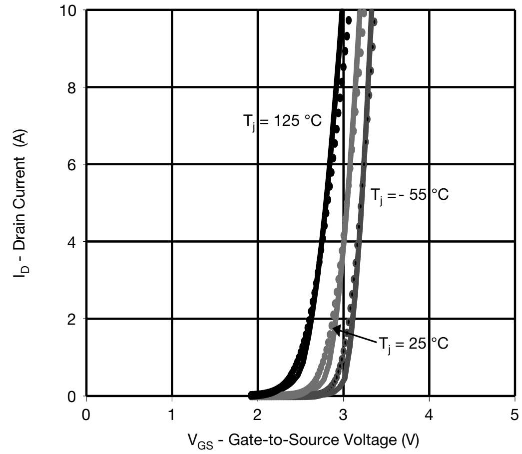
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

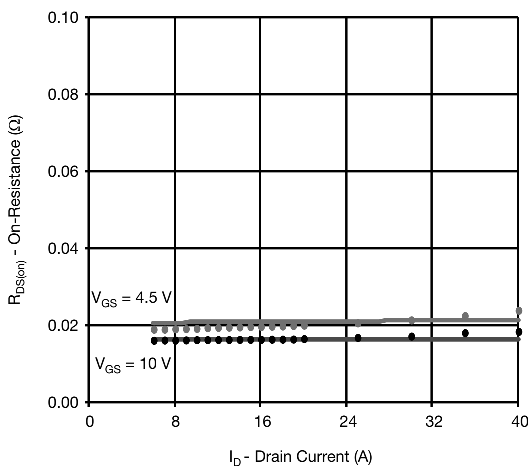
b. Guaranteed by design, not subject to production testing.

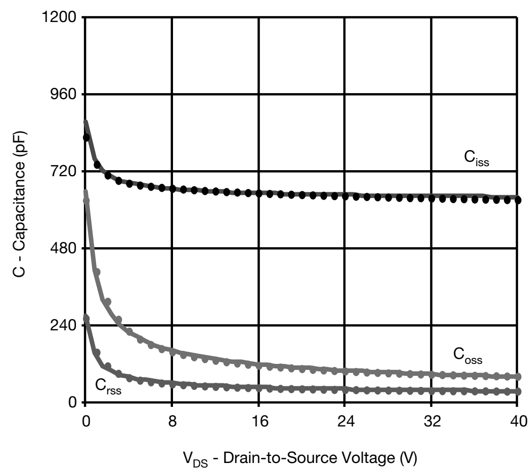
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

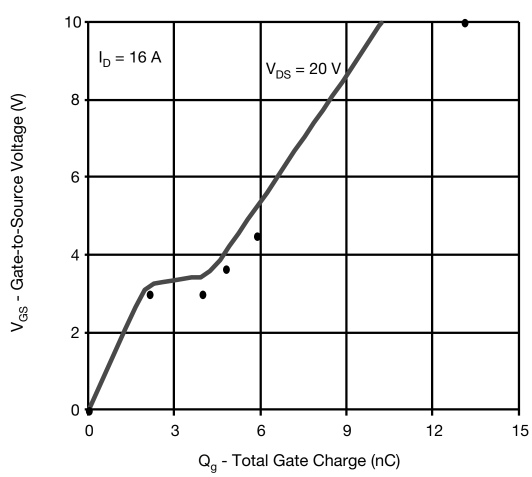
N-Channel 1 MOSFET

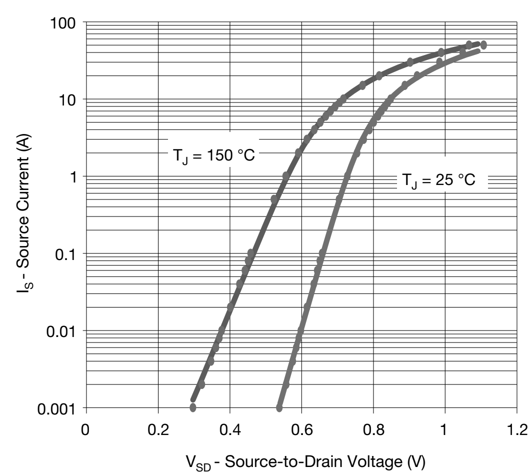










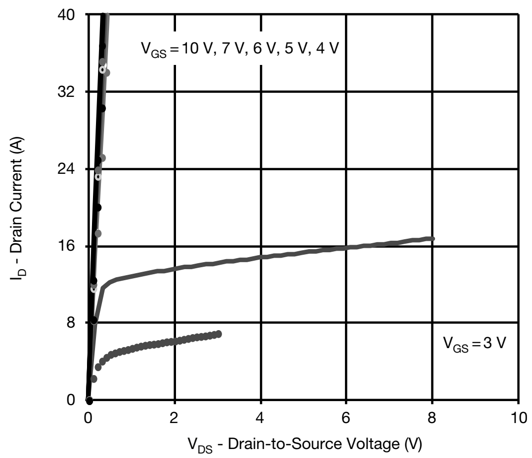


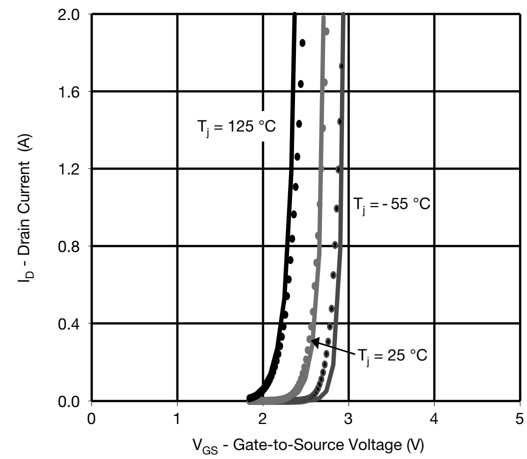
Note

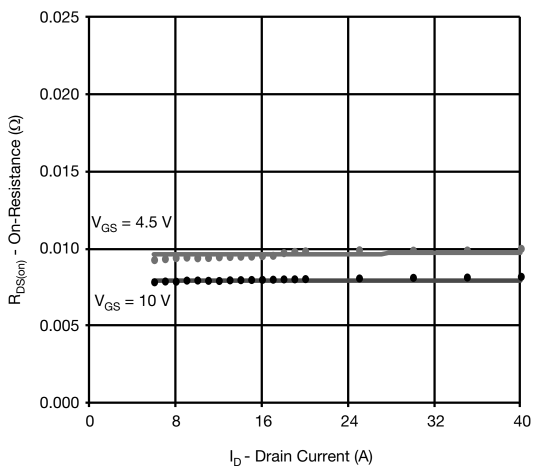
- Dots and squares represent measured data.

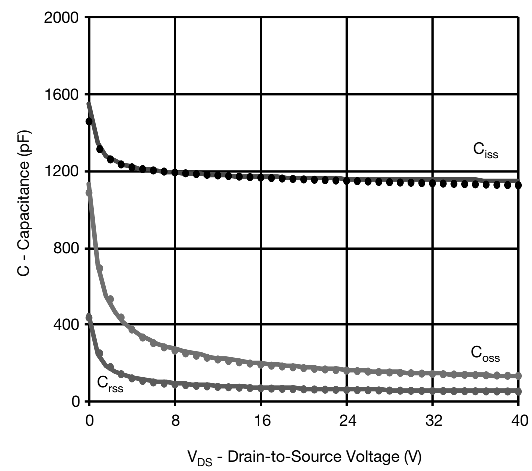
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

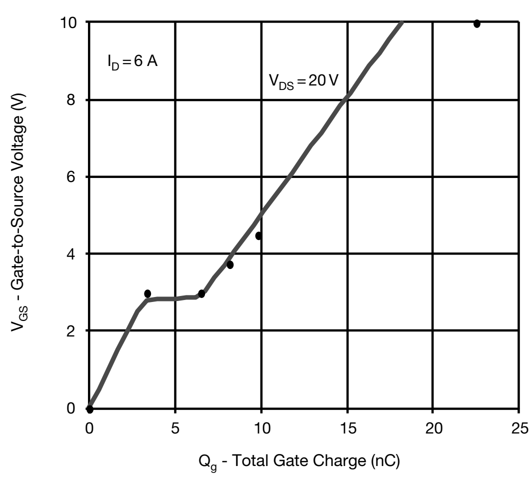
N-Channel 2 MOSFET

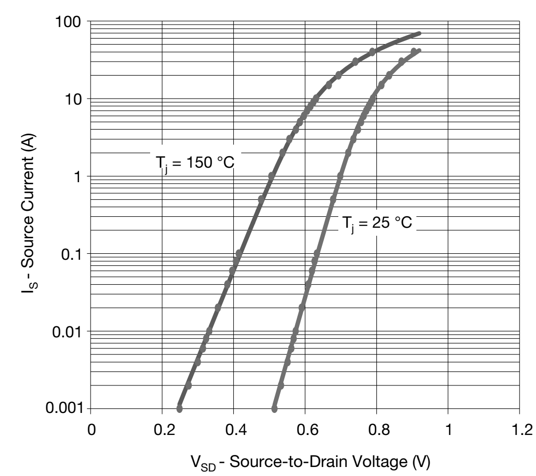












Note

- Dots and squares represent measured data.

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