Vishay Siliconix



# N-Channel 150 V (D-S) MOSFET

## **DESCRIPTION**

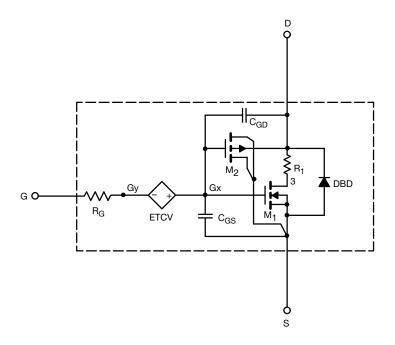
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## **CHARACTERISTICS**

- N-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- · Model the Gate Charge

## SUBCIRCUIT MODEL SCHEMATIC



### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



# **SPICE Device Model SiA446DJ**

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SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	-	V
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$	0.135	0.145	Ω
		$V_{GS} = 6 \text{ V}, I_{D} = 1 \text{ A}$	0.160	0.165	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3 A	6	6	S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 3.5 A	0.90	0.90	V
Dynamic <sup>b</sup>					
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V, f = 1 MHz	226	230	pF
Output Capacitance	Coss		51	47	
Reverse Transfer Capacitance	C <sub>rss</sub>		7.4	8	
Total Gate Charge	Qg	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 3.5 \text{ A}$	4.3	5.3	nC
		$V_{DS} = 75 \text{ V}, V_{GS} = 7.5 \text{ V}, I_{D} = 3.5 \text{ A}$	3.5	4.3	
Gate-Source Charge	Q <sub>gs</sub>		1.2	1.2	
Gate-Drain Charge	Q <sub>gd</sub>		1.8	1.8	

#### Notes

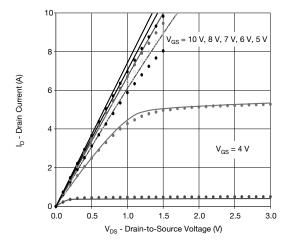
a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$ 

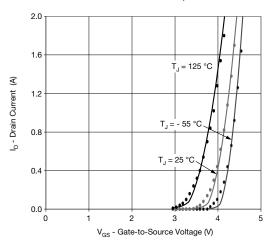
b. Guaranteed by design, not subject to production testing.

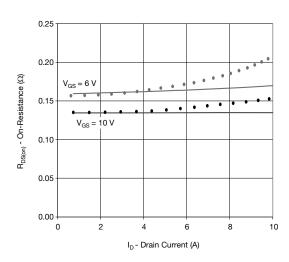
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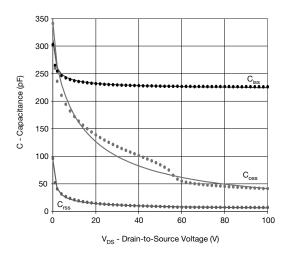
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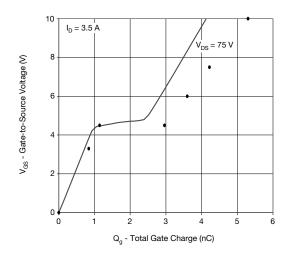
## **COMPARISON OF MODEL WITH MEASURED DATA** ( $T_J = 25$ °C, unless otherwise noted)

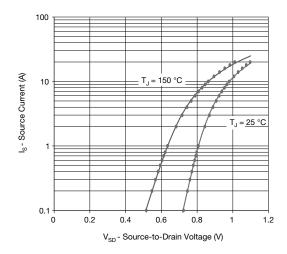












#### Note

• Dots and squares represent measured data. Copyright: Vishay Intertechnology, Inc.



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