SPICE Device Model SiR470DP



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N-Channel 40 V (D-S) MOSFET

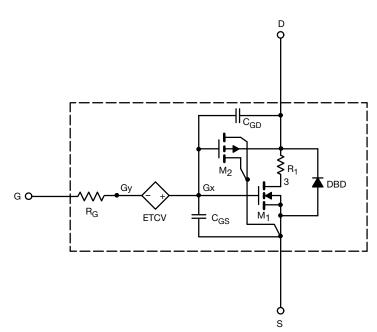
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - $55 \degree$ C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge



SUBCIRCUIT MODEL SCHEMATIC

Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

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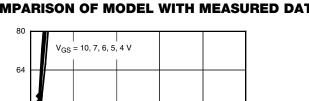
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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.7	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	0.0019	0.0019	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	0.0023	0.0222	
Forward Transconductance ^a	9fs	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	170	190	S
Diode Forward Voltage	V _{SD}	I _S = 5 A	0.73	0.73	V
Dynamic ^b					
Input Capacitance	C _{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	5680	5660	pF
Output Capacitance	C _{oss}		751	720	
Reverse Transfer Capacitance	C _{rss}		334	327	
Total Gate Charge	0	$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	89	102	nC
	Qg		43	45.5	
Gate-Source Charge	Q _{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	13.8	13.8	
Gate-Drain Charge	Q _{gd}		14.4	14.4	

Notes

a. Pulse test; pulse width $\leq 300~\mu\text{s},$ duty cycle $\leq 2~\%.$

b. Guaranteed by design, not subject to production testing.



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SHA

= - 55 °C

T_J = 125

°C

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Ciss

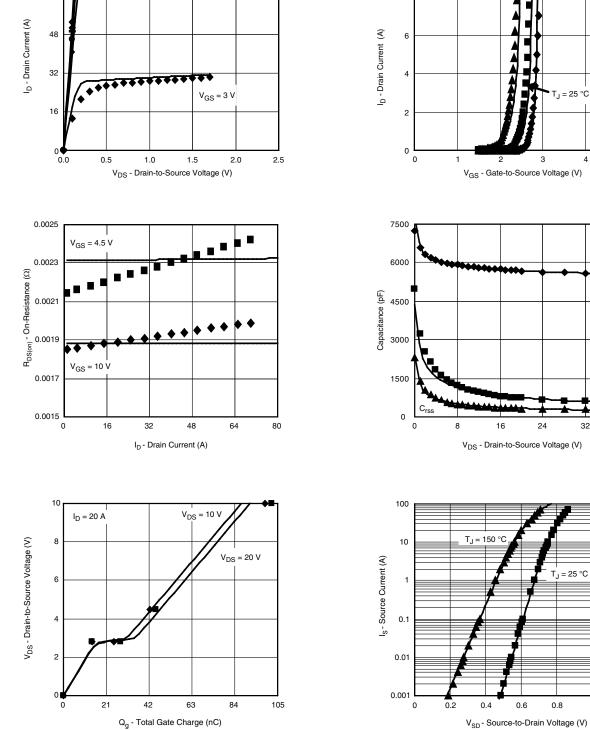
 C_{oss}

40

COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

10

8



Note

· Dots and squares represent measured data.

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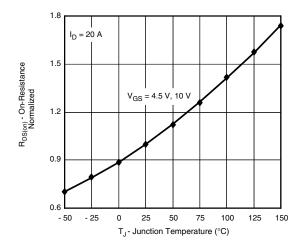
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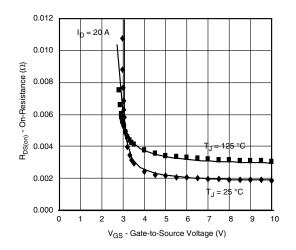
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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)





Note

• Dots and squares represent measured data.

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