



Dual N-Channel 30-V (D-S) MOSFET with Schottky Diode

CHARACTERISTICS

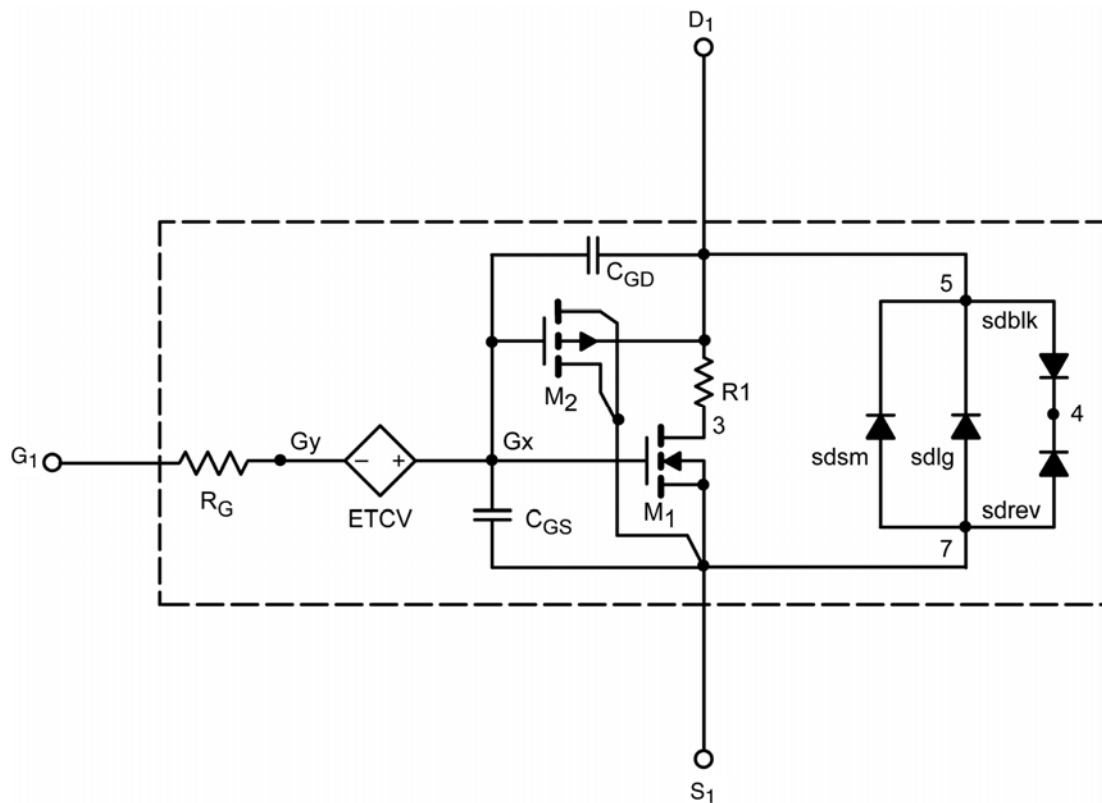
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the N-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



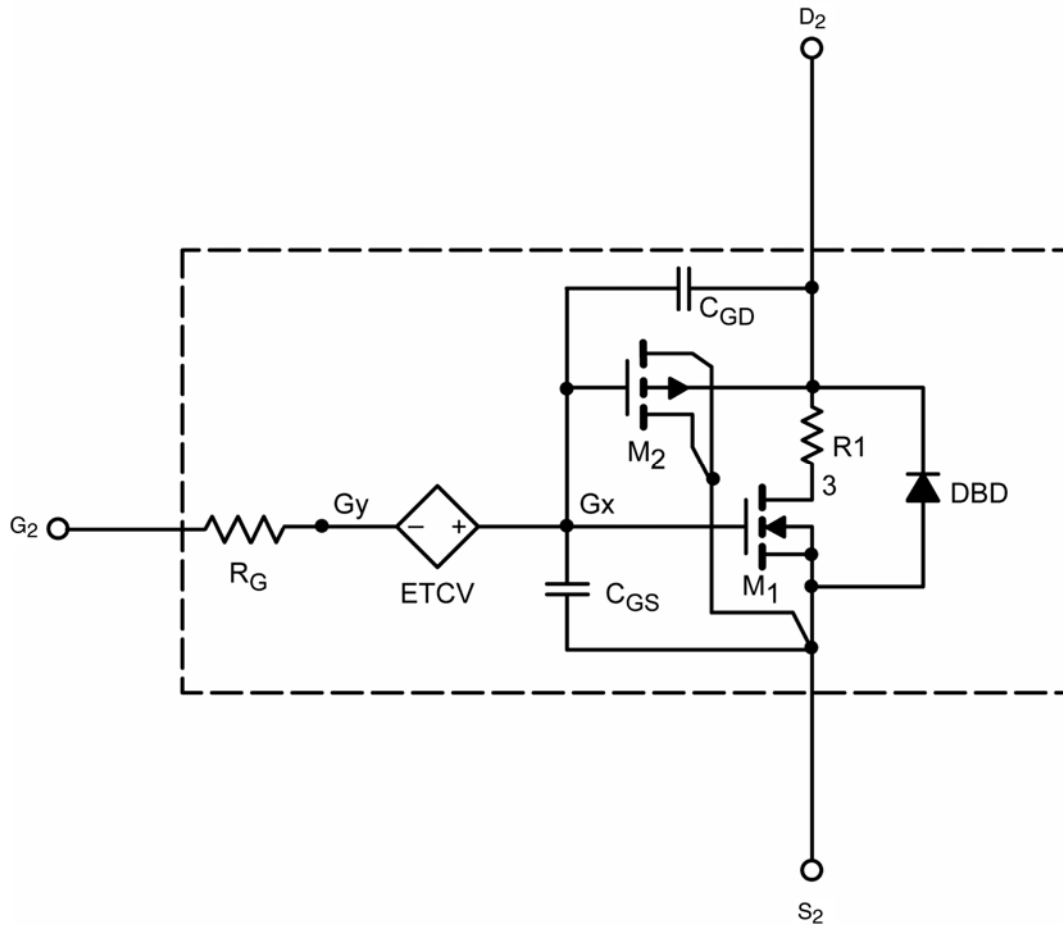
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model Si4834CDY



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SUBCIRCUIT MODEL SCHEMATIC





SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit	
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1.8		V
			Ch-2	1.8		
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$	Ch-1	0.0154	0.0156	Ω
			Ch-2	0.0154	0.0156	
			Ch-1	0.020	0.019	
			Ch-2	0.020	0.019	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 8\text{ A}$	Ch-1	29	29	S
			Ch-2	29	29	
Diode Forward Voltage ^a	V_{SD}	$I_S = 1\text{ A}$	Ch-1	0.45	0.46	V
			Ch-2	0.74	0.74	
Dynamic^b						
Input Capacitance	C_{iss}	Channel 1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ Channel 2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	945	950	pF
			Ch-2	945	950	
Input Capacitance	C_{oss}		Ch-1	184	185	
			Ch-2	184	155	
Reverse Transfer Capacitance	C_{rss}		Ch-1	64	65	
			Ch-2	64	65	
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 8\text{ A}$	Ch-1	14	16.5	nC
			Ch-2	14	16.5	
			Ch-1	7	7.3	
			Ch-2	7	7.3	
Gate-Source Charge	Q_{gs}	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$ Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$	Ch-1	2.7	2.7	
			Ch-2	2.7	2.7	
Gate-Drain Charge	Q_{gd}		Ch-1	2.1	2.1	
			Ch-2	2.1	2.1	

Notes

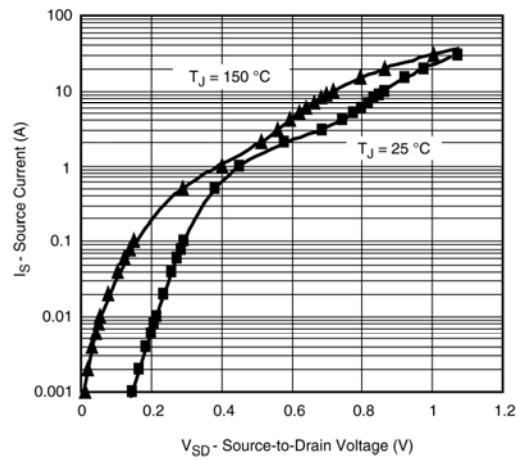
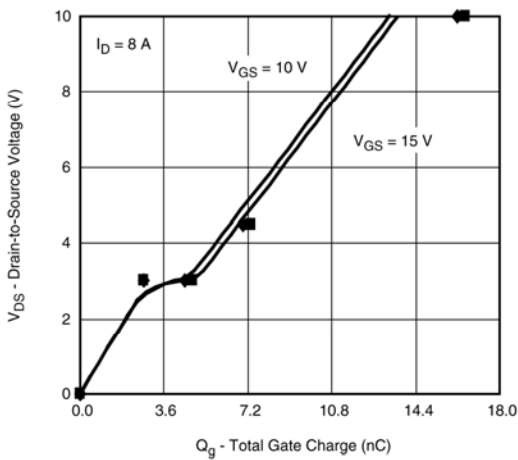
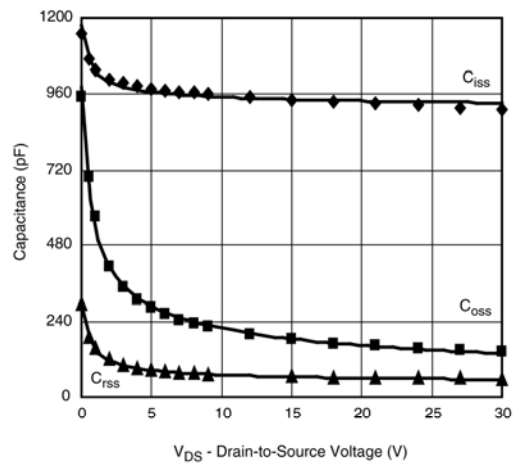
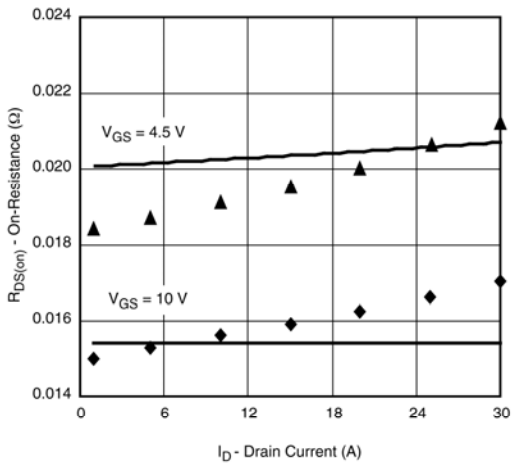
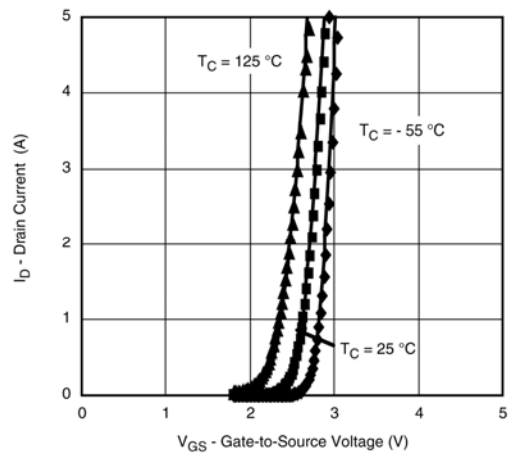
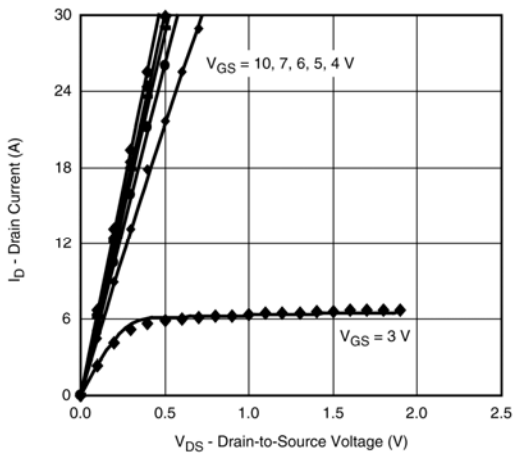
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

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CHANNEL 1 - COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)



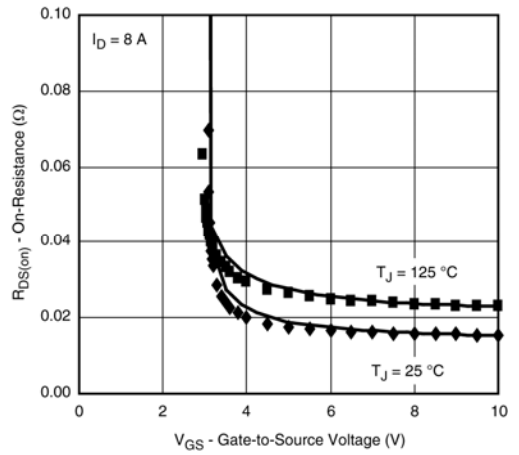
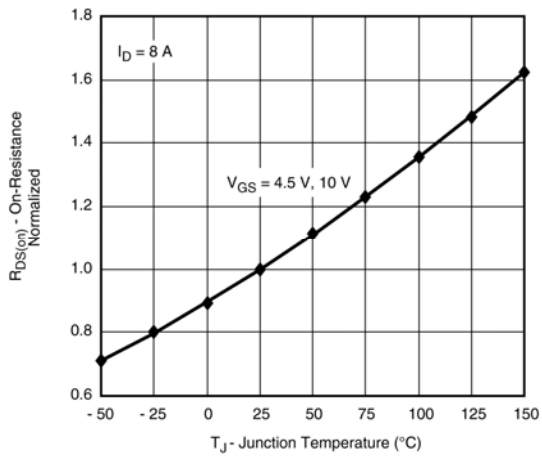
Note: Dots and squares represent measured data.



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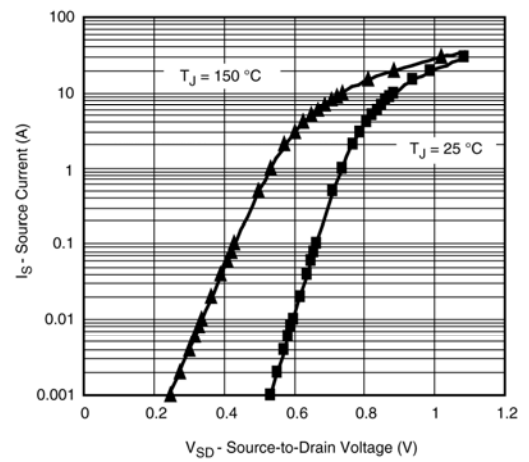
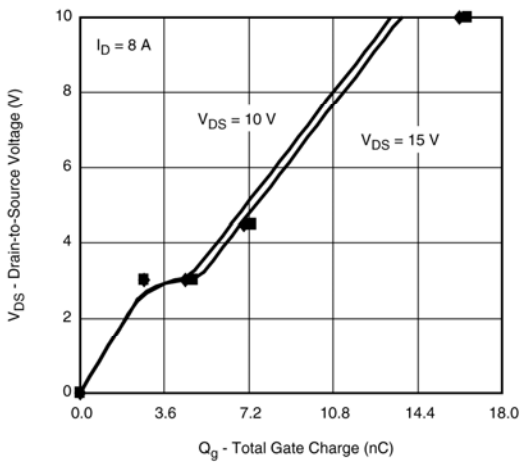
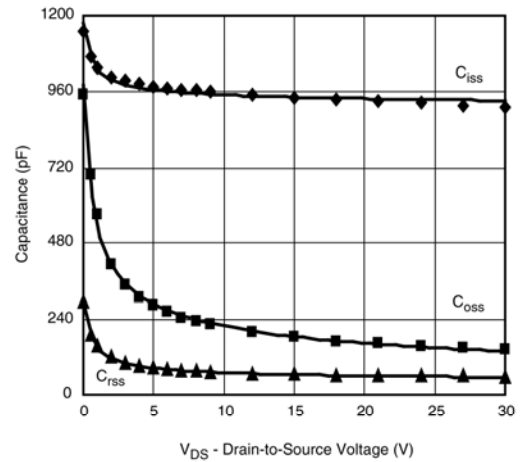
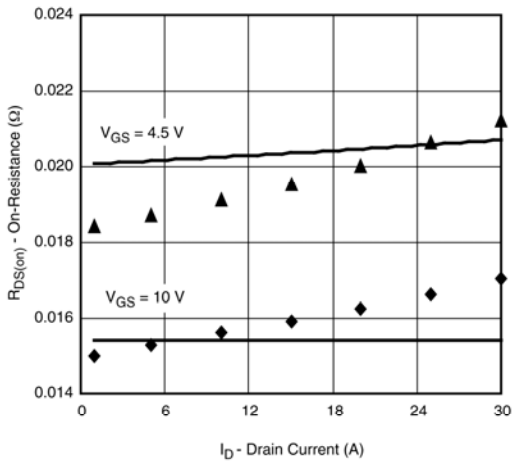
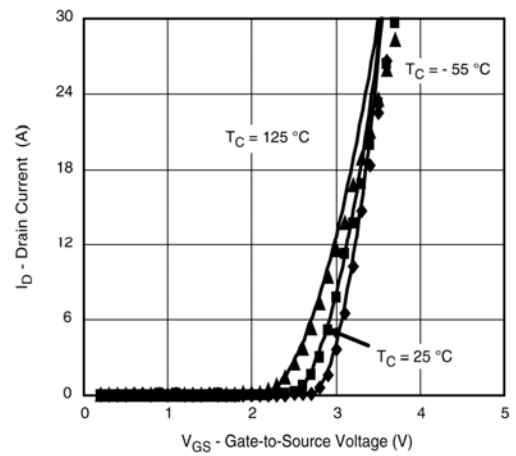
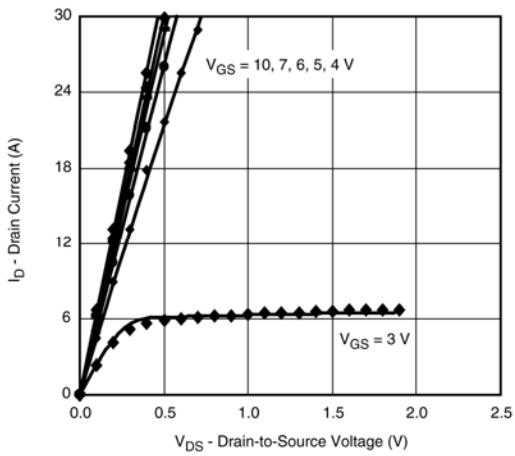
CHANNEL 1 - COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



CHANNEL 2 - COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)



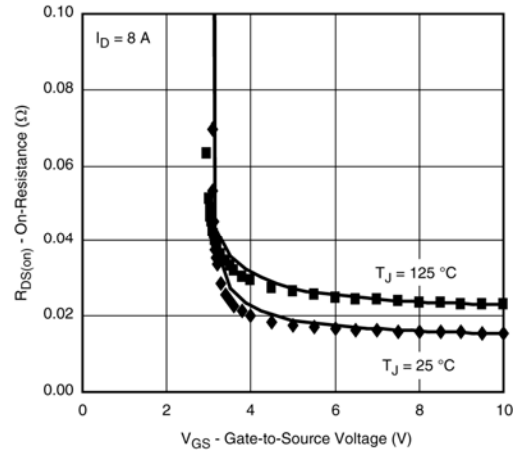
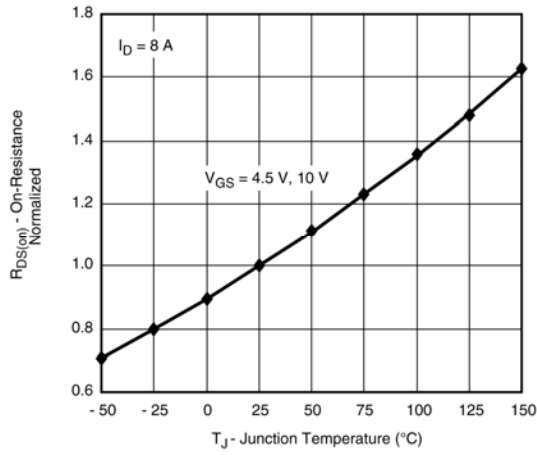
Note: Dots and squares represent measured data.



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CHANNEL 2 - COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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