

Vishay Siliconix

# N-Channel 30 V (D-S) MOSFET

### **DESCRIPTION**

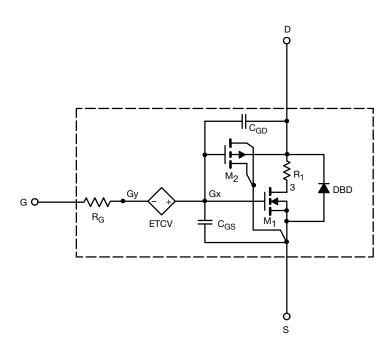
The attached spice model describes the typical electrical characteristics of the N-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### **CHARACTERISTICS**

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### SUBCIRCUIT MODEL SCHEMATIC



### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



# **SPICE Device Model Si7114ADN**

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SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.8	-	V
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 18 \text{ A}$	0.0064	0.0062	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 16 \text{ A}$	0.0085	0.0081	
Forward Transconductancea	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_D = 18 \text{ A}$	70	50	S
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A	0.80	0.80	V
Dynamic <sup>b</sup>					
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	1220	1230	pF
Output Capacitance	C <sub>oss</sub>		276	275	
Reverse Transfer Capacitance	C <sub>rss</sub>		104	105	
Total Gate Charge	Qg	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 18 A	19	21	nC
		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 18 A	10	10.2	
Gate-Source Charge	$Q_{gs}$		3.9	3.9	
Gate-Drain Charge	Q <sub>gd</sub>		3.2	3.2	

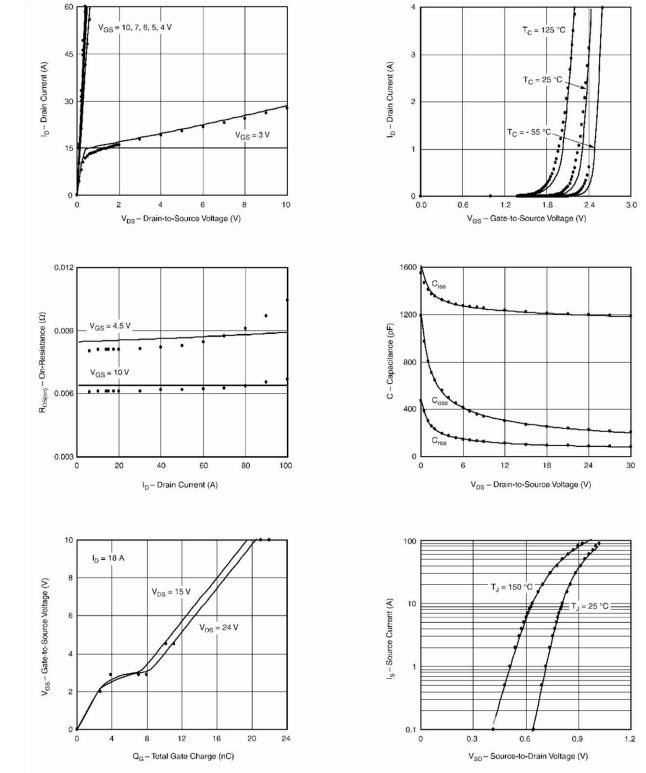
#### **Notes**

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

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## **COMPARISON OF MODEL WITH MEASURED DATA** ( $T_J = 25~^{\circ}C$ , unless otherwise noted)



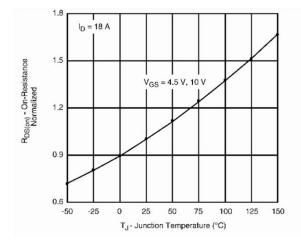
#### Note

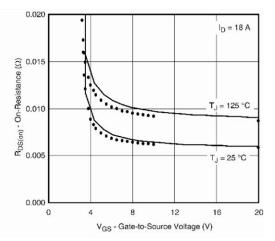
• Dots and squares represent measured data.

# **SPICE Device Model Si7114ADN**

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## **COMPARISON OF MODEL WITH MEASURED DATA** ( $T_J = 25$ °C, unless otherwise noted)





#### Note

• Dots and squares represent measured data.



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