

P-Channel 20 V (D-S) MOSFET

DESCRIPTION

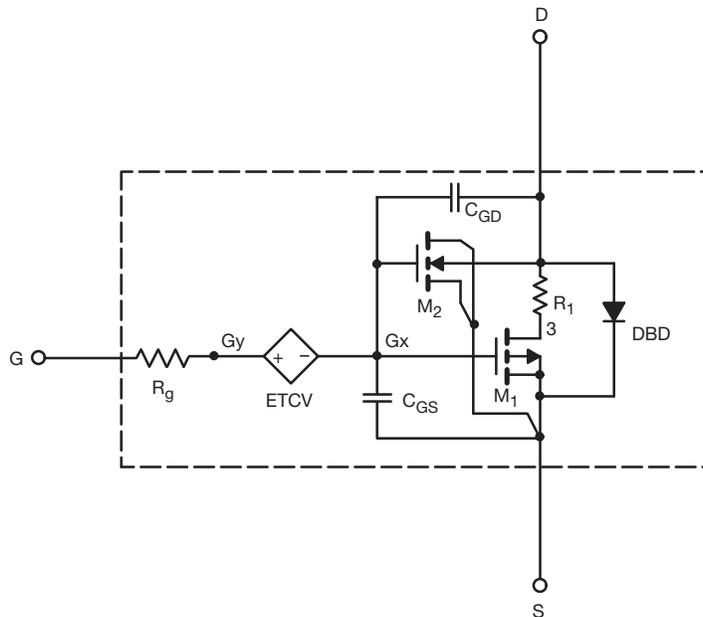
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the $-55\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the $-55\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



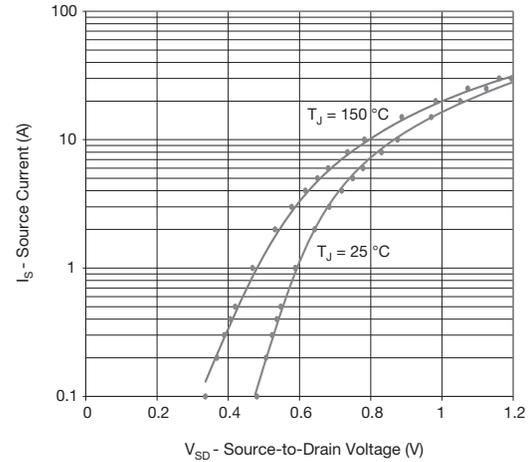
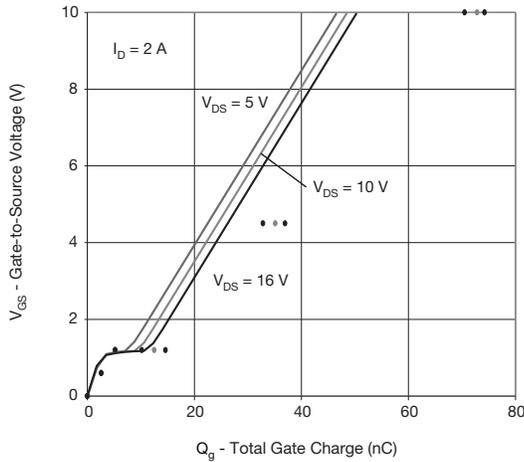
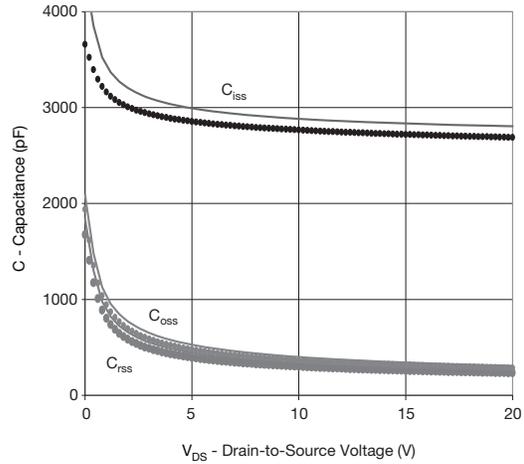
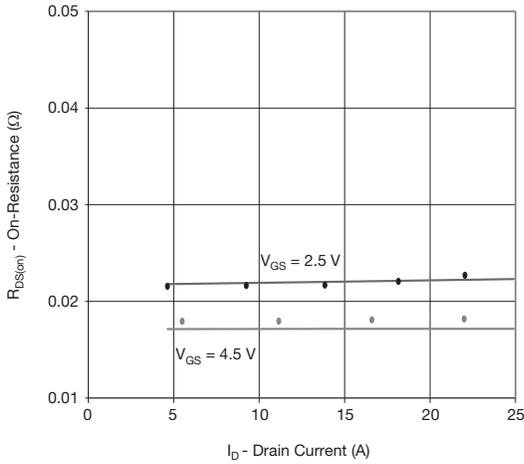
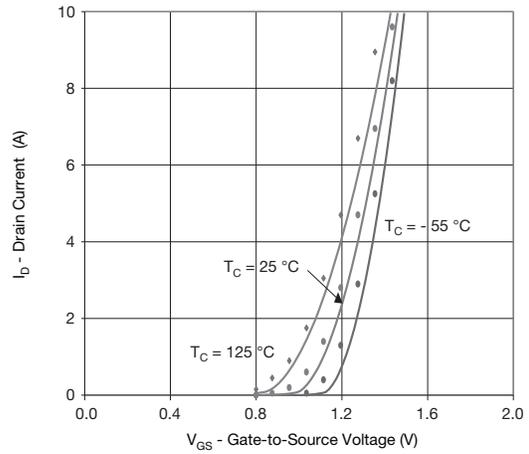
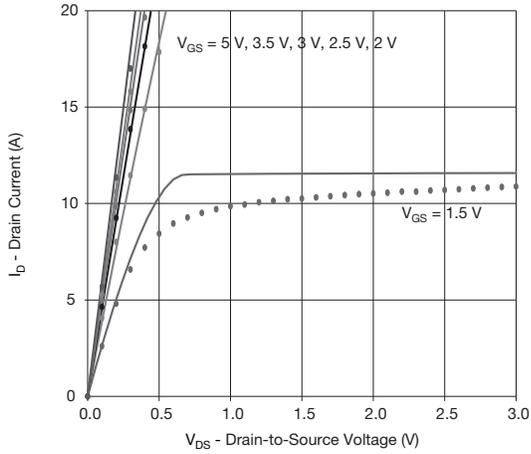
| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | |
|--|--------------|---|----------------|---------------|----------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$ | 0.7 | - | V |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = -4.5\ \text{V}, I_D = -2\ \text{A}$ | 0.017 | 0.018 | Ω |
| | | $V_{GS} = -2.5\ \text{V}, I_D = -1\ \text{A}$ | 0.022 | 0.021 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = -10\ \text{V}, I_D = -2\ \text{A}$ | 18 | 18 | S |
| Diode Forward Voltage | V_{SD} | $I_S = -2\ \text{A}$ | -0.7 | -0.7 | V |
| Dynamic ^b | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = -10\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$ | 2880 | 2800 | pF |
| Output Capacitance | C_{oss} | | 400 | 370 | |
| Reverse Transfer Capacitance | C_{rss} | | 336 | 305 | |
| Total Gate Charge | Q_g | $V_{DS} = -10\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -2\ \text{A}$ | 50 | 73 | nC |
| | | $V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -2\ \text{A}$ | 25 | 36 | |
| Gate-Source Charge | Q_{gs} | | 5.2 | 5.2 | |
| Gate-Drain Charge | Q_{gd} | | 7.3 | 7.3 | |

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ \%$.
b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

• Dots and squares represent measured data.

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