

N- and P-Channel 20 V (D-S) MOSFET

DESCRIPTION

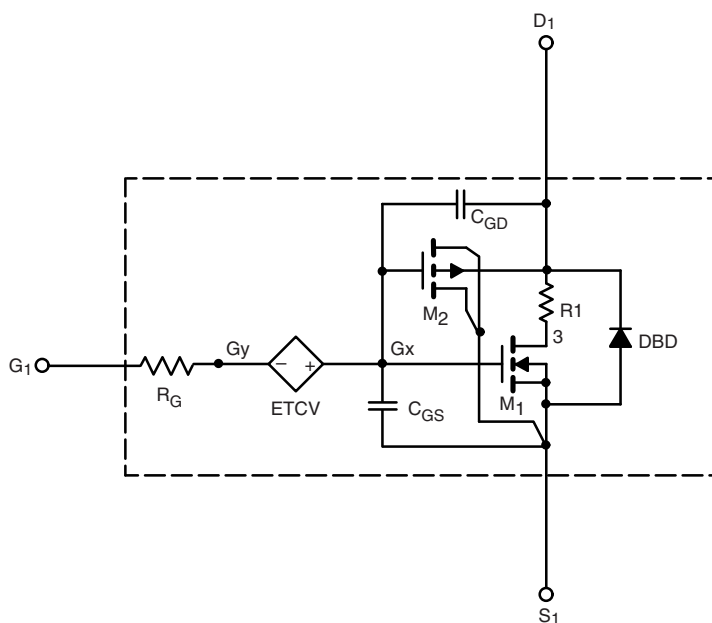
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC N-CHANNEL

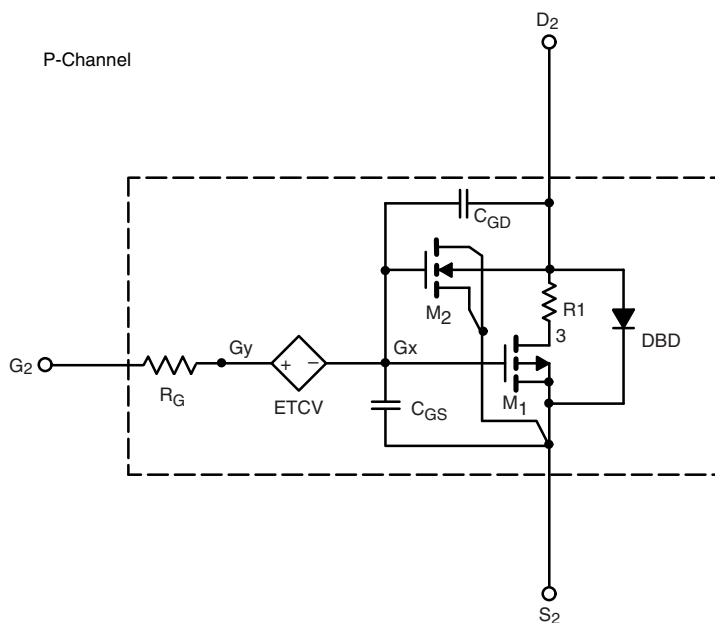


Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SUBCIRCUIT MODEL SCHEMATIC P-CHANNEL



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT	
Static							
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1	-	V	
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	1	-		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.4 A	N-Ch	0.044	0.045	Ω	
		V _{GS} = - 4.5 V, I _D = - 2.4 A	P-Ch	0.12	0.12		
		V _{GS} = 2.5 V, I _D = 3.6 A	N-Ch	0.067	0.065		
		V _{GS} = - 2.5 V, I _D = - 1.9 A	P-Ch	0.200	0.204		
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 4.4 A	N-Ch	10	12	S	
		V _{DS} = - 10 V, I _D = - 2.4 A	P-Ch	6	5		
Diode Forward Voltage ^a	V _{SD}	I _S = 3.5 A, V _{GS} = 0 V	N-Ch	0.83	0.80	V	
		I _S = - 1.9 A, V _{GS} = 0 V	P-Ch	0.81	- 0.80		
Dynamic ^b							
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	278	285	pF	
			P-Ch	250	252		
Output Capacitance	C _{oss}		P-Channel V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	62		65
				P-Ch	62		62
Reverse Transfer Capacitance	C _{rss}		N-Ch	29	30		
			P-Ch	44	25		
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 5 V, I _D = 4.4 A	N-Ch	2.4	2.8	nC	
		V _{DS} = - 10 V, V _{GS} = - 5 V, I _D = - 2.4 A	P-Ch	3.1	3.9		
		N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 4.4 A	N-Ch	2.2	2.6		
			P-Ch	2.8	3.6		
Gate-Source Charge	Q _{gs}	P-Channel V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 2.4 A	N-Ch	0.7	0.7		
			P-Ch	0.6	0.6		
Gate-Drain Charge	Q _{gd}		N-Ch	0.5	0.5		
			P-Ch	1.2	1.2		

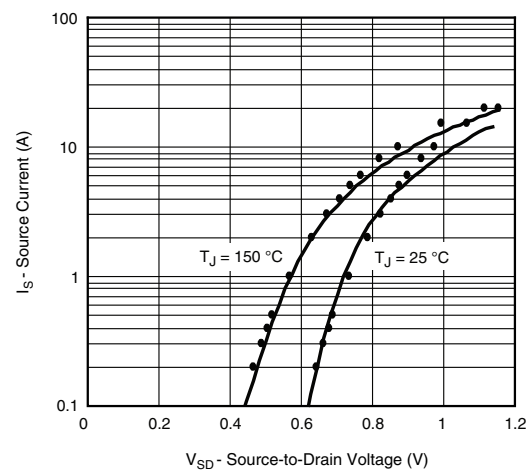
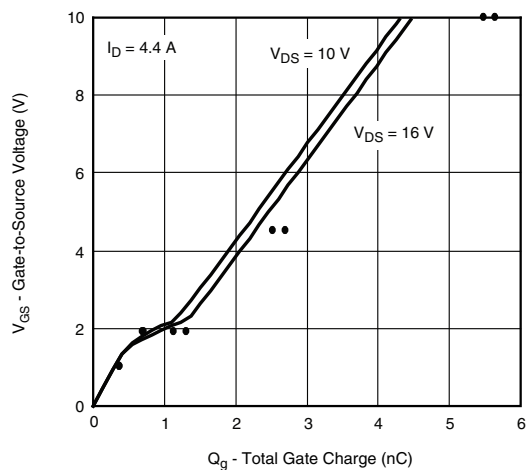
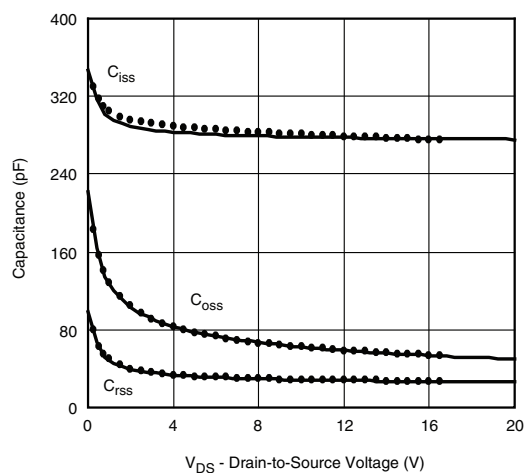
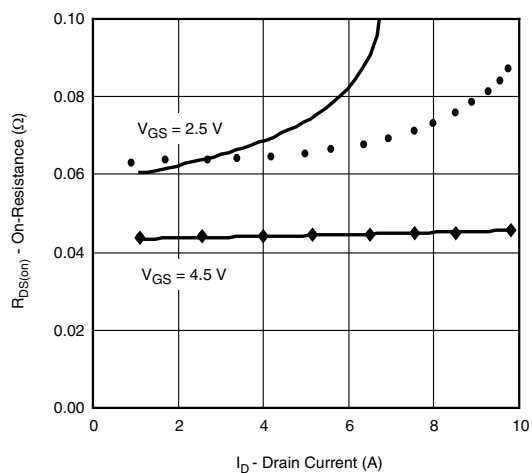
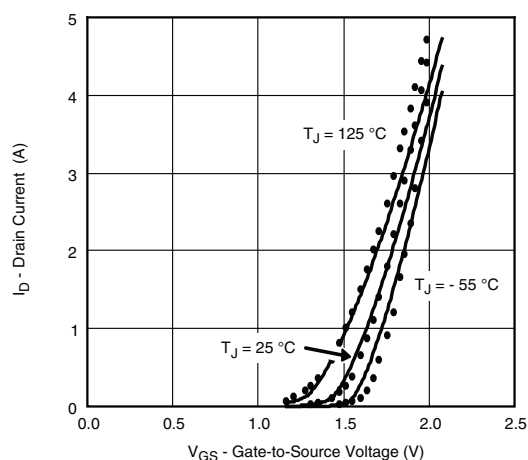
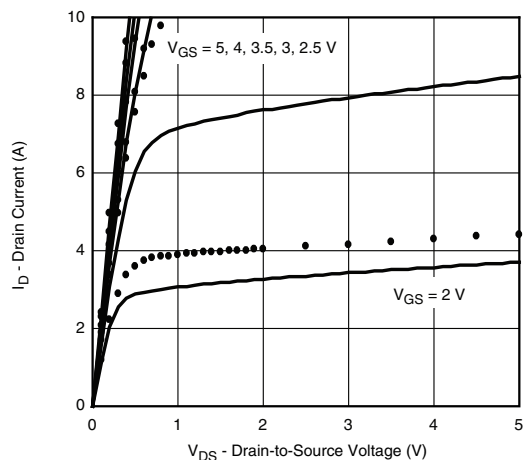
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

N-Channel MOSFET



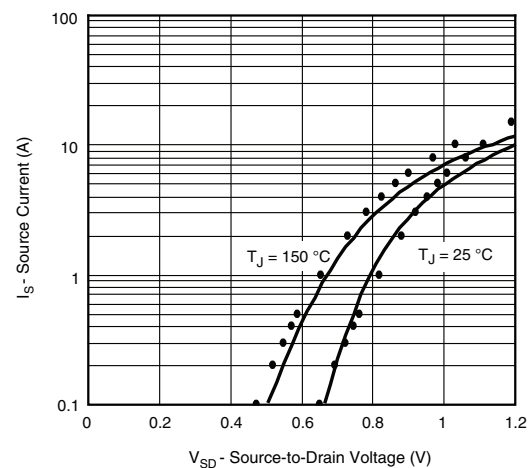
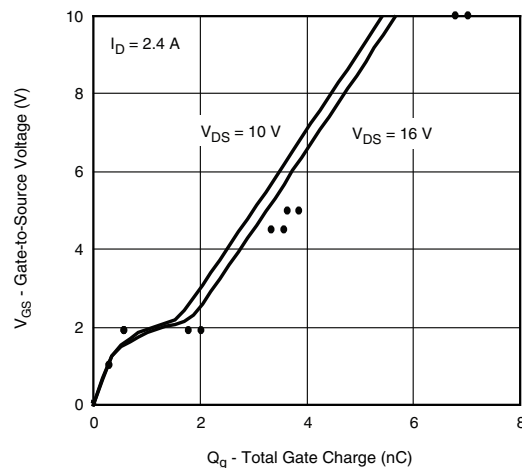
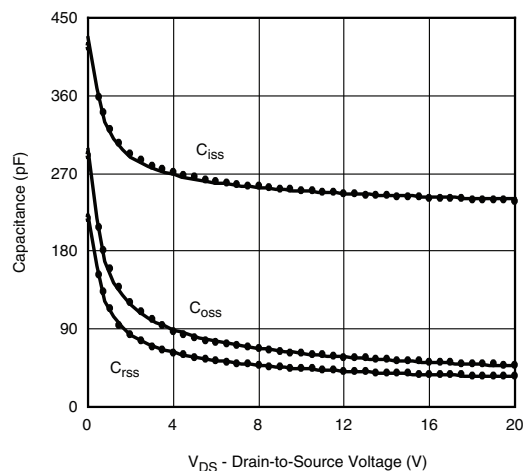
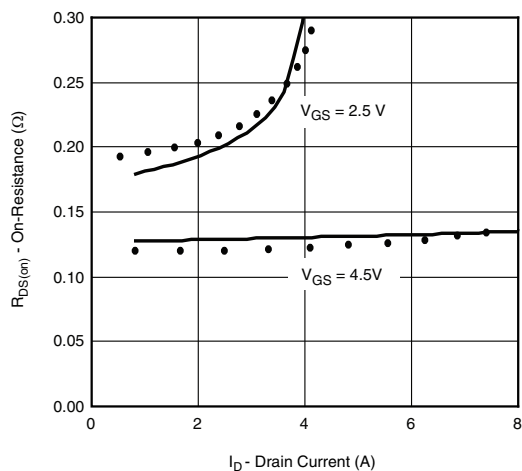
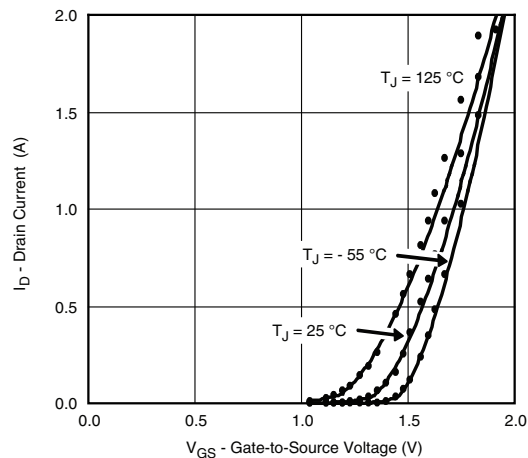
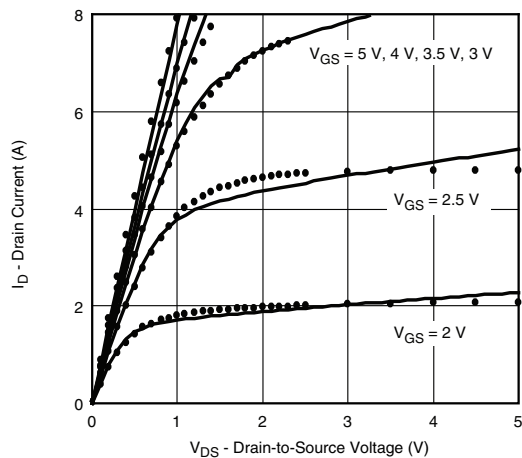
Note

- Dots and squares represent measured data.



COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25^\circ\text{C}$, unless otherwise noted

P-Channel MOSFET



Note

- Dots and squares represent measured data.