SPICE Device Model SiS436DN



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N-Channel 25 V (D-S) MOSFET

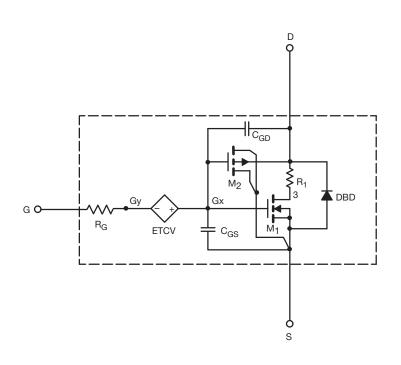
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge



Note

 This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

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| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | |
|--|---------------------|--|-------------------|------------------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | $V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$ | 2.1 | - | V |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | $V_{GS} = 10 \text{ V}, \text{ I}_{D} = 10 \text{ A}$ | 0.0084 | 0.0085 | Ω |
| | | V_{GS} = 4.5 V, I_D = 7 A | 0.0106 | 0.0105 | |
| Forward Transconductance ^a | g fs | $V_{DS} = 15 \text{ V}, \text{ I}_{D} = 10 \text{ A}$ | 24 | 45 | S |
| Diode Forward Voltage | V _{SD} | I _S = 3 A | 0.79 | 0.80 | V |
| Dynamic ^b | | | | | |
| Input Capacitance | C _{iss} | V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz | 847 | 855 | pF |
| Output Capacitance | C _{oss} | | 259 | 255 | |
| Reverse Transfer Capacitance | C _{rss} | | 96 | 95 | |
| Total Gate Charge | Qg | $V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$ | 13.3 | 14.3 | nC |
| | | V_{DS} = 10 V, V_{GS} = 4.5 V, I_{D} = 10 A | 6.6 | 6.7 | |
| Gate-Source Charge | Q _{gs} | | 2 | 2 | |
| Gate-Drain Charge | Q _{gd} | | 1.8 | 1.8 | |

Notes

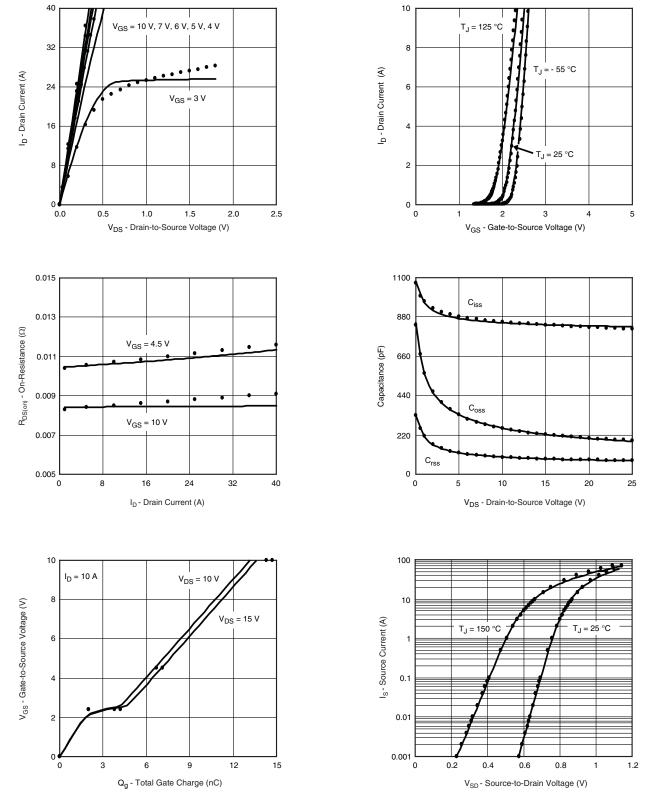
a. Pulse test; pulse width $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%.$

b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data.

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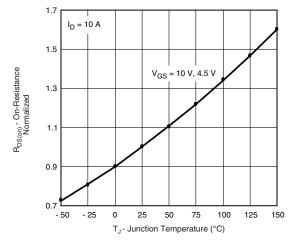
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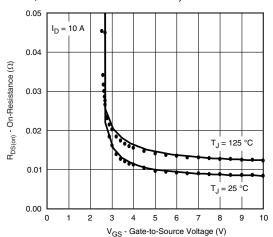
Document Number: 64795



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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)





Note

• Dots and squares represent measured data.



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