

Dual N-Channel 30 V (D-S) MOSFET with Schottky Diode

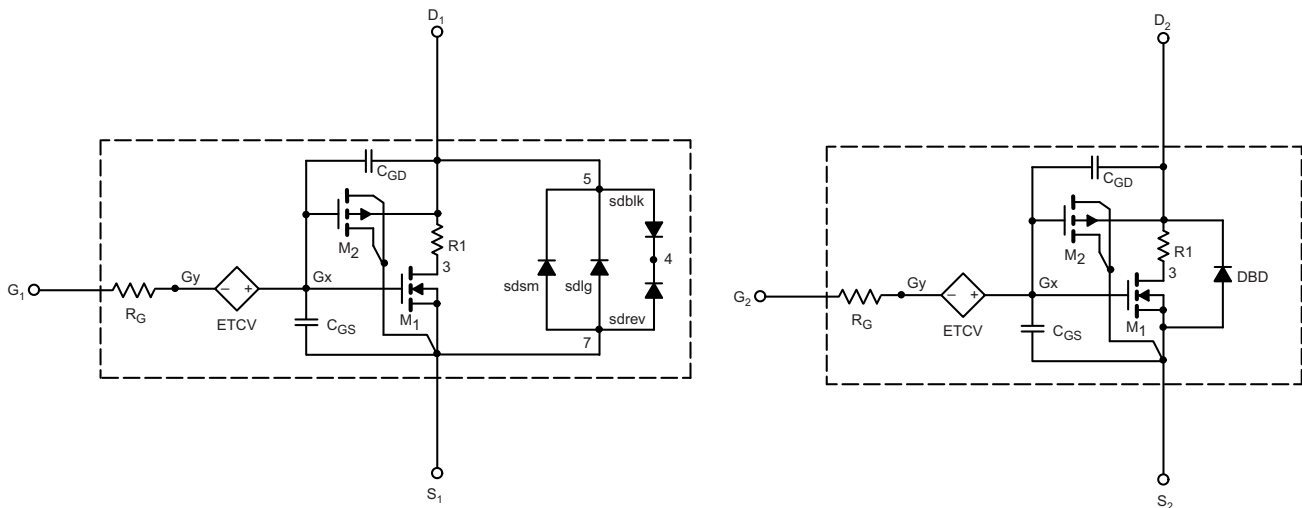
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

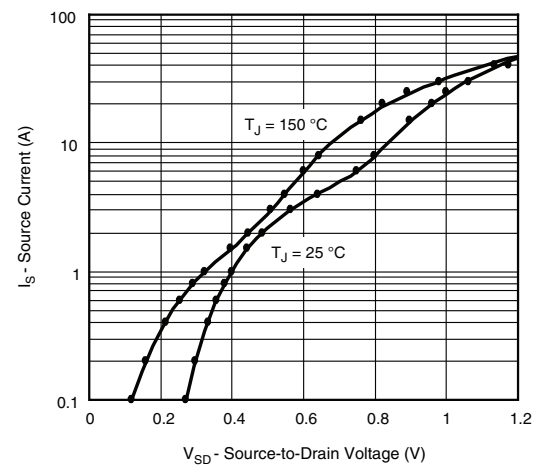
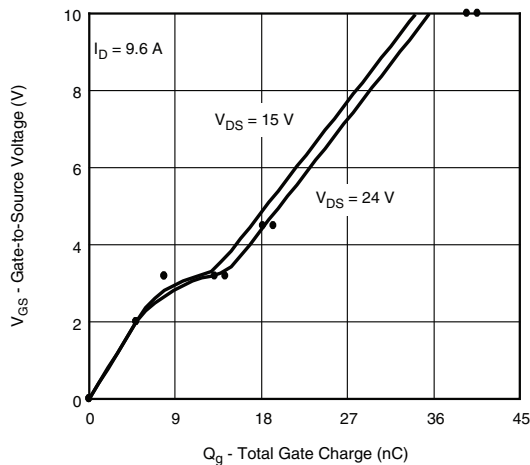
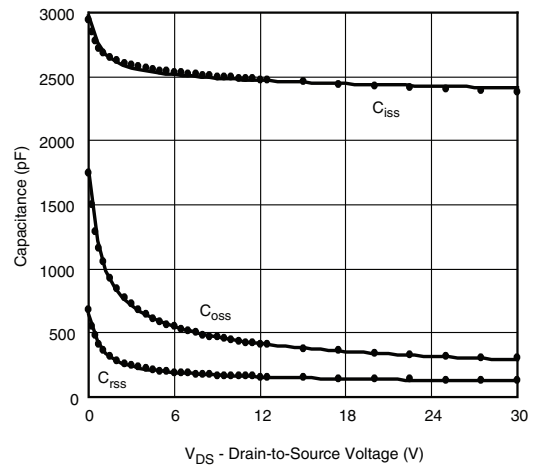
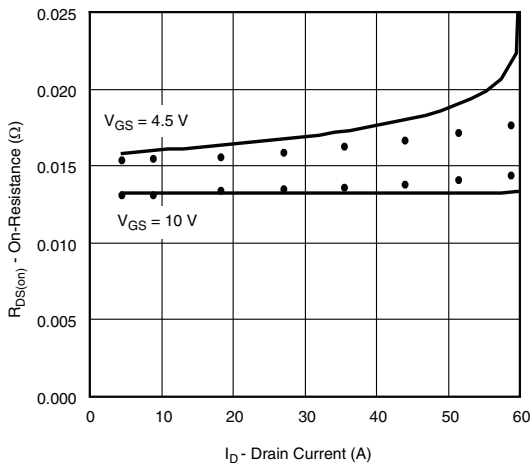
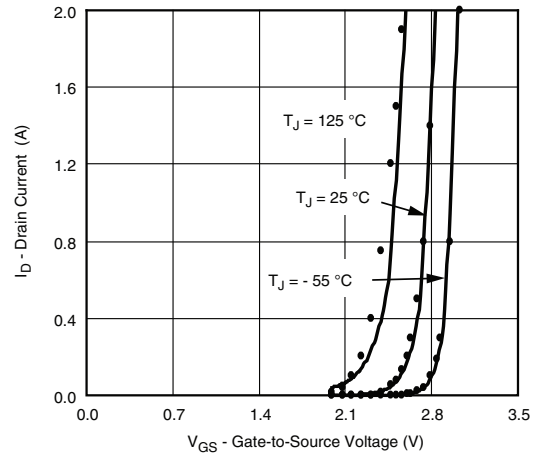
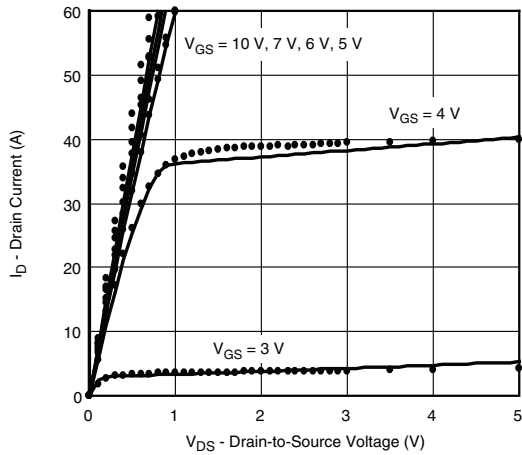
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	2	-	V	
			Ch-2	1.4	-		
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 9.6\text{ A}$	Ch-1	0.0132	0.0132	Ω	
			Ch-2	0.021	0.022		
			$V_{GS} = 4.5\text{ V}, I_D = 8.9\text{ A}$	Ch-1	0.016		0.0155
				Ch-2	0.024		0.024
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 9.6\text{ A}$	Ch-1	28	94	S	
			Ch-2	23	10		
Diode Forward Voltage ^a	V_{SD}	$I_S = 7.7\text{ A}$	Ch-1	0.48	0.57	V	
			Ch-2	0.82	0.80		
Dynamic^b							
Input Capacitance	C_{iss}	Channel 1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	Ch-1	2460	2458	pF	
			Ch-2	761	760		
Output Capacitance	C_{oss}	Channel 2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	Ch-1	384	385	pF	
			Ch-2	109	110		
Reverse Transfer Capacitance	C_{rss}	Channel 1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	Ch-1	148	150	pF	
			Ch-2	47	50		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 9.6\text{ A}$	Ch-1	35	40	nC	
			Ch-2	12	13.2		
Gate-Source Charge	Q_{gs}	Channel 1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 9.6\text{ A}$	Ch-1	17	19	nC	
			Ch-2	6	6		
Gate-Drain Charge	Q_{gd}	Channel 2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 6.7\text{ A}$	Ch-1	8	8	nC	
			Ch-2	2.1	2.1		
Gate-Drain Charge	Q_{gd}	Channel 2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 6.7\text{ A}$	Ch-1	6	6	nC	
			Ch-2	1.4	1.4		

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted

Channel 1

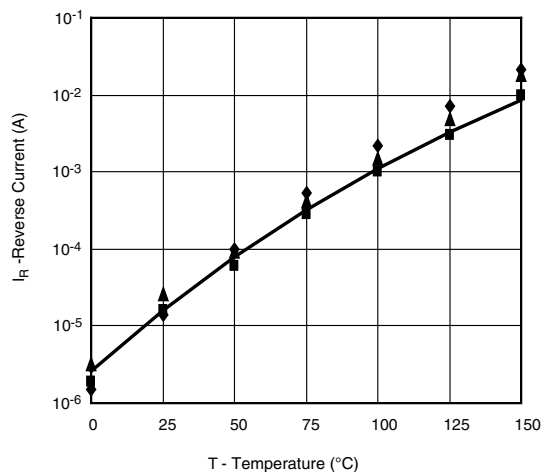
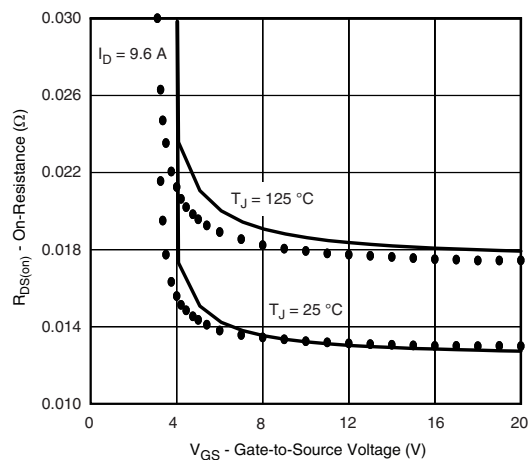
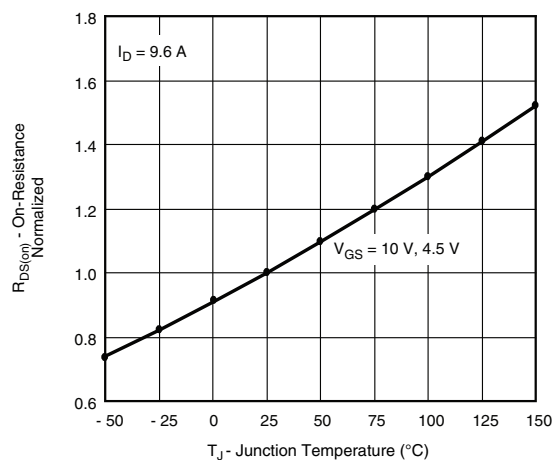


Note

Dots and squares represent measured data.

COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted

Channel 1



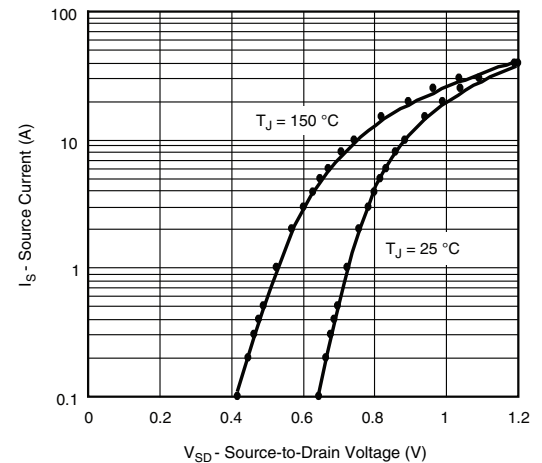
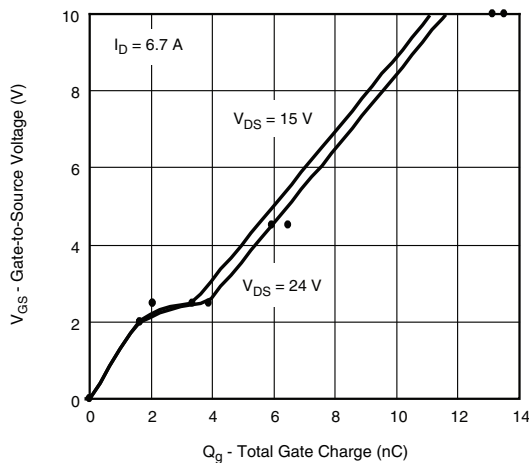
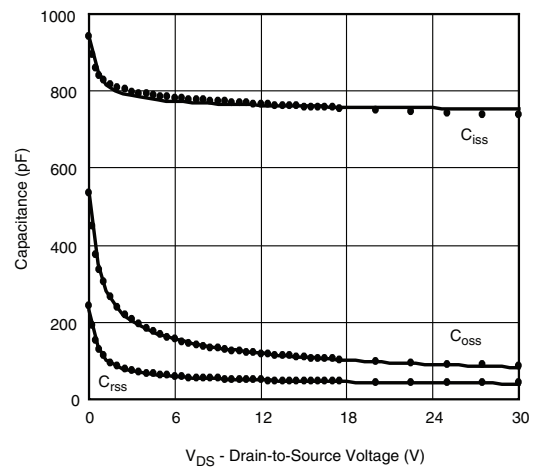
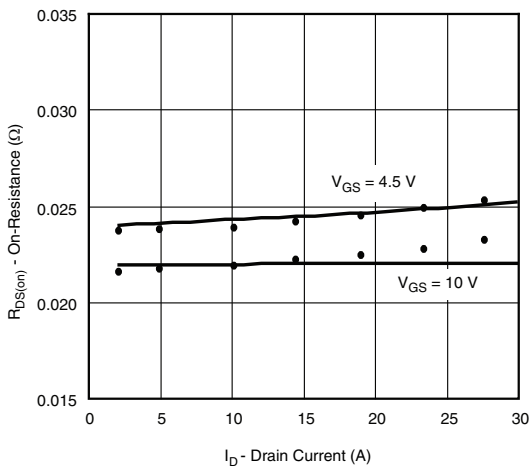
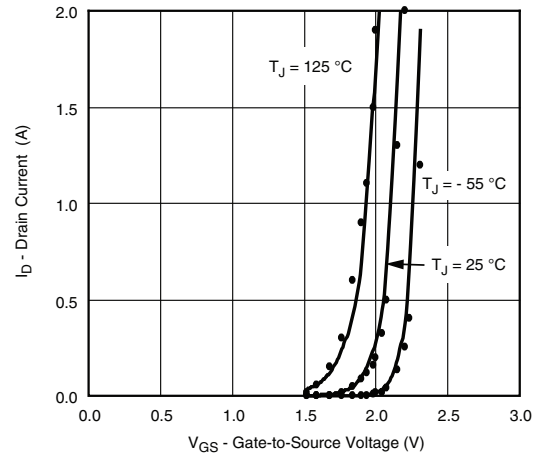
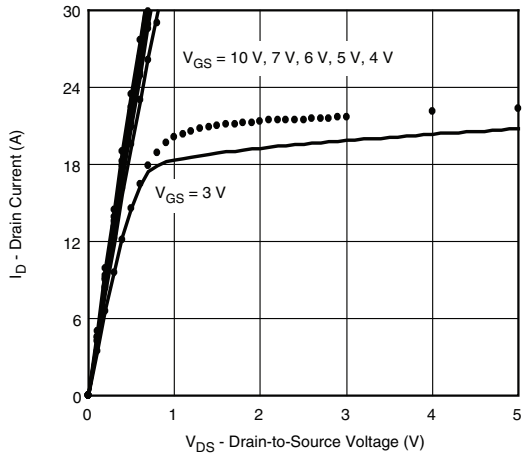
Note

Dots and squares represent measured data.



COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted

Channel 2



Note

Dots and squares represent measured data.



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