COMPLIANT

HALOGEN FREE





N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY							
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)				
30	0.013 at V _{GS} = 10 V	14.6	8.3 nC				
30	0.0165 at $V_{GS} = 4.5$ V	12.9	0.5110				

SO-8 S 1 8 D S 2 7 D S 3 6 D Top View

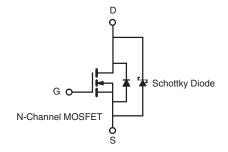
Ordering Information: Si4712DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- SkyFET[®] Monolithic TrenchFET[®] Power MOSFET and Schottky Diode
- 100 % R_g Tested
- 100 % UIS Tested
- · Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Notebook System Power
 - Low Side



Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	30	V		
Gate-Source Voltage	V_{GS}	± 20	ľ		
	T _C = 25 °C		14.6		
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C	1_	11.6	Ī	
Continuous Diam Current (1) = 130 °C)	T _A = 25 °C	I _D	10.3 ^{b, c}		
	T _A = 70 °C		8.2 ^{b, c}	_	
Pulsed Drain Current	I _{DM}	50	Α		
Continuous Source-Drain Diode Current	T _C = 25 °C	l _a	4.5		
Continuous Source-Drain Diode Current	T _A = 25 °C	ls -	2.3 ^{b, c}		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	15		
Single Pulse Avalanche Energy	L = 0.1 mn	E _{AS}	11.25	mJ	
	T _C = 25 °C		5		
Maximum Power Dissipation	T _C = 70 °C	P _D	3.2	w	
Maximum Fower Dissipation	T _A = 25 °C	' D	2.5 ^{b, c}	VV	
	T _A = 70 °C		1.6 ^{b, c}	İ	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Тур.	Max.	Unit		
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	38	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	20	25	0, 11		

Notes:

- a. Based on $T_C = 25$ °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s
- d. Maximum under Steady State conditions is 85 °C/W.

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SPECIFICATIONS $T_J = 25 ^{\circ}C$,	unicoo our	1					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	ı				T T		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	30			V	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 1 \text{ mA}$	1.2		2.5		
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$		0.028	0.2 mA		
Zoro date Voltage Brain Gurrent	.022	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 100 ^{\circ}\text{C}$		2	20		
On -State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Durin Course On Otata Basistana a	В	V _{GS} = 10 V, I _D = 15 A		0.0105	0.013	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		0.013	0.0165		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 15 A		37		S	
Dynamic ^b							
Input Capacitance	C _{iss}			1084		pF	
Output Capacitance	C _{oss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		200			
Reverse Transfer Capacitance	C _{rss}	1		77			
Total Oats Observe		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A		18.5	28	nC	
Total Gate Charge	Q _g			8.3	12.5		
Gate-Source Charge	Q_{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A		2.8			
Gate-Drain Charge	Q_{gd}	1		2.0			
Gate Resistance	R_{g}	f = 1 MHz	0.3	1.2	2.4	Ω	
Turn-On Delay Time	t _{d(on)}			16	30		
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_L = 1.5 \Omega$		18	35		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		15	30		
Fall Time	t _f	-		10	20		
Turn-On Delay Time	t _{d(on)}			8	16	ns	
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_1 = 1.5 \Omega$		11	22		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		17	34		
Fall Time	t _f	- 		9	18		
Drain-Source Body Diode and Schottky	Characteris	tics					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			4.5	_	
Pulse Diode Forward Current ^a	I _{SM}				50	Α	
Body Diode Voltage	V _{SD}	I _S = 1 A		0.48	0.65	V	
Body Diode Reverse Recovery Time	t _{rr}	-		17	34	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	†		7	14	nC	
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 °C$		10			
Reverse Recovery Rise Time	t _b			7		ns	

Notes:

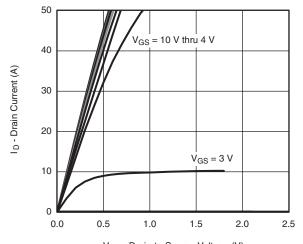
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



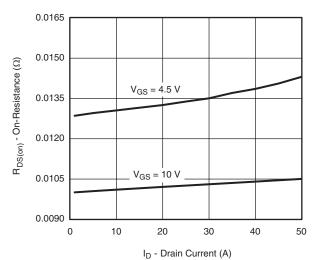


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

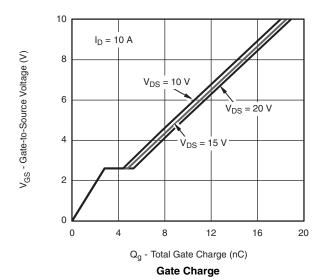


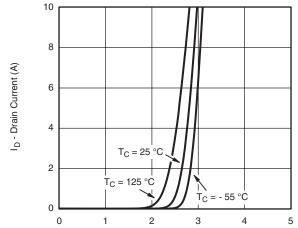
 $V_{\mbox{\scriptsize DS}}$ - Drain-to-Source Voltage (V)

Output Characteristics



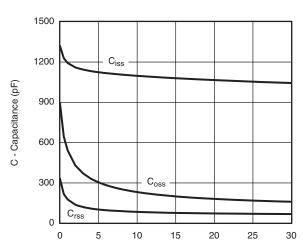
On-Resistance vs. Drain Current





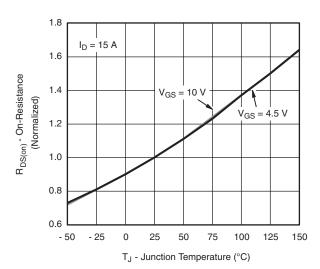
 V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics



V_{DS} - Drain-to-Source Voltage (V)

Capacitance

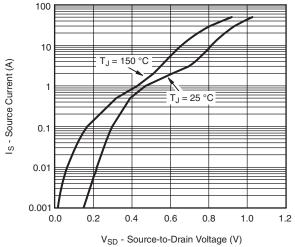


On-Resistance vs. Junction Temperature

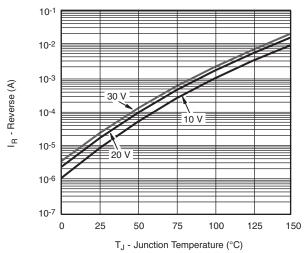
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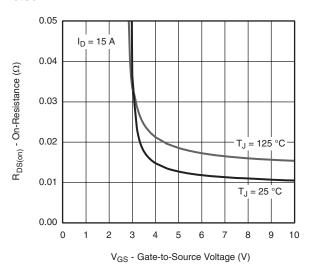
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



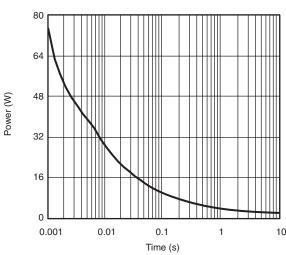




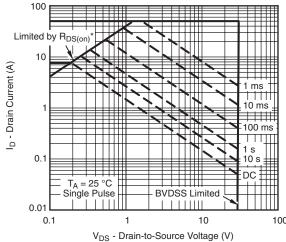
Reverse Current (Schottky)



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



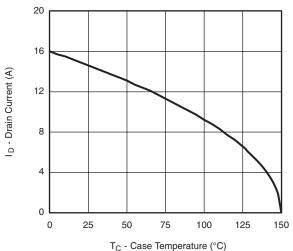
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



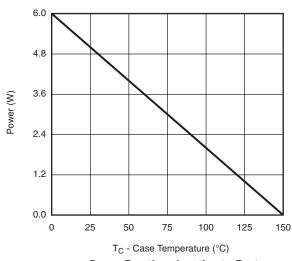


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

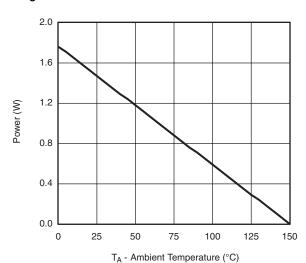


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Current Derating*







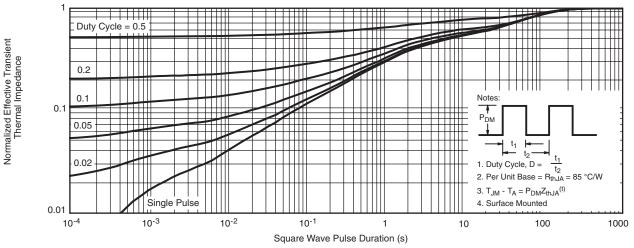
Power Derating, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

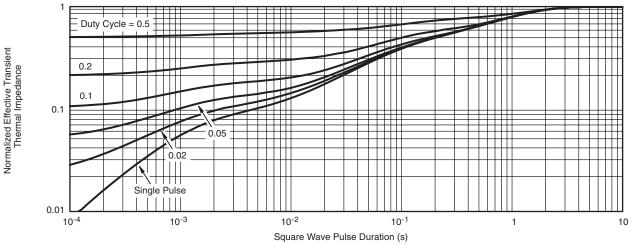
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIMETERS INCHES			HES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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