

## P-Channel 20 V (D-S) MOSFET

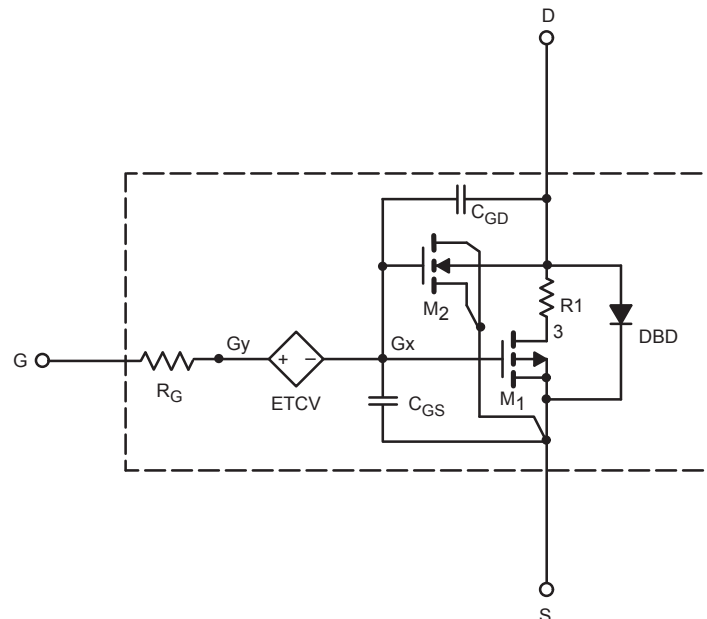
### DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



## SPECIFICATIONS (T<sub>J</sub> = 25 °C, unless otherwise noted)

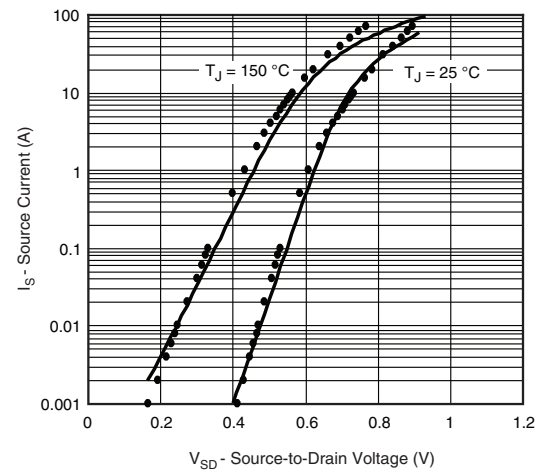
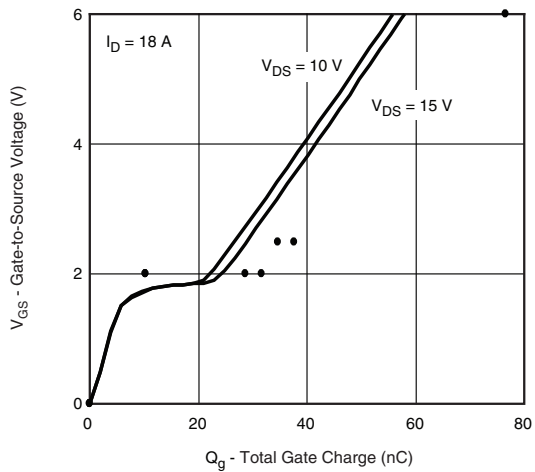
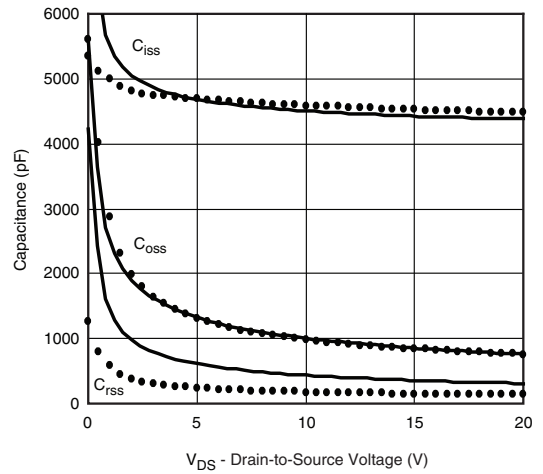
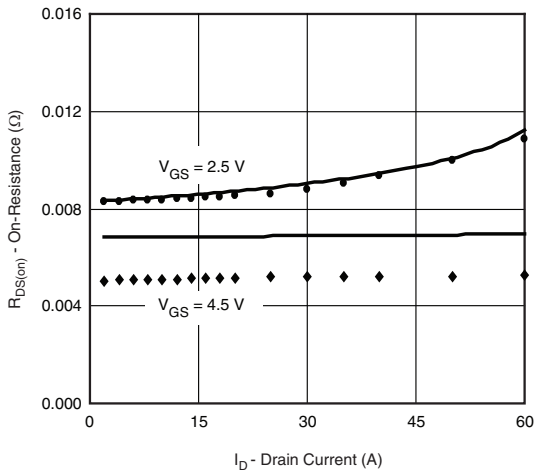
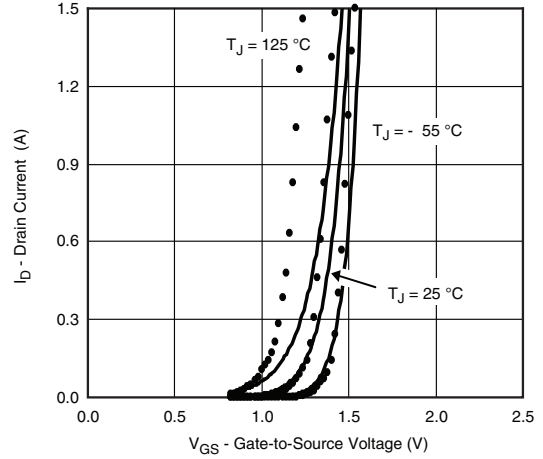
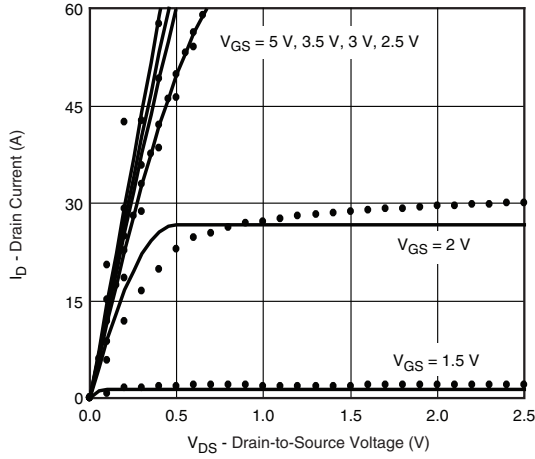
| PARAMETER                                     | SYMBOL              | TEST CONDITIONS  | SIMULATED DATA | MEASURED DATA | UNIT |
|---|---------------------|--|----------------|---------------|------|
| <b>Static</b>                                 |                     |  |                |               |      |
| Gate-Source Threshold Voltage                 | V <sub>GS(th)</sub> | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA                | 0.60           | -             | V    |
| Drain-Source On-State Resistance <sup>a</sup> | R <sub>DS(on)</sub> | V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 18 A                           | 0.0068         | 0.0051        | Ω    |
|   |                     | V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 14 A                           | 0.0085         | 0.0085        |      |
| Forward Transconductance <sup>a</sup>         | g <sub>fs</sub>     | V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 3.5 A                           | 16             | 10            | S    |
| Diode Forward Voltage <sup>a</sup>            | V <sub>SD</sub>     | I <sub>S</sub> = - 5 A   | - 0.69         | - 0.75        | V    |
| <b>Dynamic<sup>b</sup></b>                    |                     |  |                |               |      |
| Input Capacitance                             | C <sub>iss</sub>    | V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz                   | 4500           | 4600          | pF   |
| Output Capacitance                            | C <sub>oss</sub>    |  | 1010           | 980           |      |
| Reverse Transfer Capacitance                  | C <sub>rss</sub>    |  | 436            | 175           |      |
| Total Gate Charge                             | Q <sub>g</sub>      | V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 18 A  | 99             | 125           | nC   |
|   |                     | V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 18 A | 44             | 59            |      |
| Gate-Source Charge                            | Q <sub>gs</sub>     |  | 10             | 10            |      |
| Gate-Drain Charge                             | Q <sub>gd</sub>     |  | 19             | 19            |      |

### Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data.



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