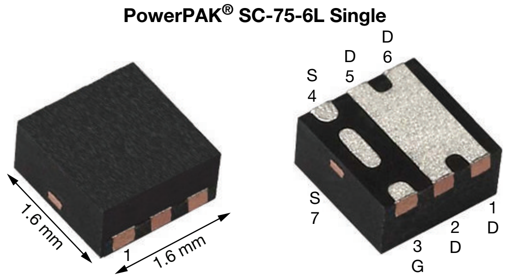
N-Channel 20 V (D-S) MOSFET

PowerPAK® SC-75-6L Single



Top View   Bottom View

Marking code: AF

FEATURES

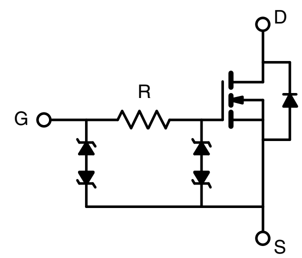
- TrenchFET® power MOSFET
- Thermally enhanced PowerPAK® SC-75 package
  - Small footprint area
  - Low on-resistance
  - Thin 0.75 mm profile
- Typical ESD protection 4000 V
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Portable devices
  - Load switch
  - Battery switch



PRODUCT SUMMARY	
V_{DS} (V)	20
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.030
$R_{DS(on)}$ max. (Ω) at V_{GS} = 2.5 V	0.041
$R_{DS(on)}$ max. (Ω) at V_{GS} = 1.8 V	0.057
$R_{DS(on)}$ max. (Ω) at V_{GS} = 1.5 V	0.082
Q_g typ. (nC)	6
I_D (A) [a]	9
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SC-75
Lead (Pb)-free and halogen-free	SiB422EDK-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GS}	± 8	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	9 [a]	A
	T_C = 70 °C		9 [a]	
	T_A = 25 °C		7.1 [b, c]	
	T_A = 70 °C		5.7 [b, c]	
Pulsed drain current		I_{DM}	25	
Continuous source-drain diode current	T_C = 25 °C	I_S	9 [a]	
	T_A = 25 °C		2.1 [b, c]	
Maximum power dissipation	T_C = 25 °C	P_D	13	W
	T_C = 70 °C		8.4	
	T_A = 25 °C		2.5 [b, c]	
	T_A = 70 °C		1.6 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [b, f]	t ≤ 5 s	R_{thJA}	41	51	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	7.5	9.5	

Notes

a. Package limited, T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 5 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 105 °C/W

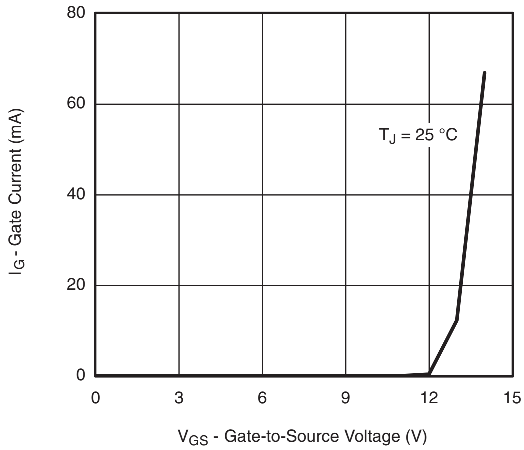
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	-	18	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-2.5	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	0.4	-	1.0	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V	-	-	± 1.5	µA
		V_{DS} = 0 V, V_{GS} = ± 8 V	-	-	± 25	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	-	-	1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C	-	-	10	
On-state drain current [a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 4.5 V	15	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 5 A	-	0.025	0.030	Ω
		V_{GS} = 2.5 V, I_D = 4.3 A	-	0.034	0.041	
		V_{GS} = 1.8 V, I_D = 1.5 A	-	0.046	0.057	
		V_{GS} = 1.5 V, I_D = 1 A	-	0.055	0.082	
Forward transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 5 A	-	28	-	S
Dynamic [b]						
Total gate charge	Q_g	V_{DS} = 10 V, V_{GS} = 8 V, I_D = 7.1 A	-	11.5	18	nC
		V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 7.1 A	-	6	9	
Gate-source charge	Q_{gs}		-	0.8	-	
Gate-drain charge	Q_{gd}		-	1.6	-	
Gate resistance	R_g	f = 1 MHz	460	2300	4600	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 1.8 Ω $I_D \cong$ 5.7 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	0.3	0.45	µs
Rise time	t_r		-	0.6	0.9	
Turn-off delay time	$t_{d(off)}$		-	3.8	6	
Fall time	t_f		-	1.7	2.6	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 1.8 Ω $I_D \cong$ 5.7 A, V_{GEN} = 10 V, R_g = 1 Ω	-	0.15	0.25	
Rise time	t_r		-	0.3	0.45	
Turn-off delay time	$t_{d(off)}$		-	5.6	9	
Fall time	t_f		-	1.6	2.5	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	9	A
Pulse diode forward current	I_{SM}		-	-	25	
Body diode voltage	V_{SD}	I_S = 5.7 A, V_{GS} = 0 V	-	0.85	1.2	V
Body diode reverse recovery time	t_{rr}	I_F = 5.7 A, di/dt = 100 A/µs, T_J = 25 °C	-	15	30	ns
Body diode reverse recovery charge	Q_{rr}		-	7.5	15	nC
Reverse recovery fall time	t_a		-	8	-	ns
Reverse recovery rise time	t_b		-	15	-	

Notes

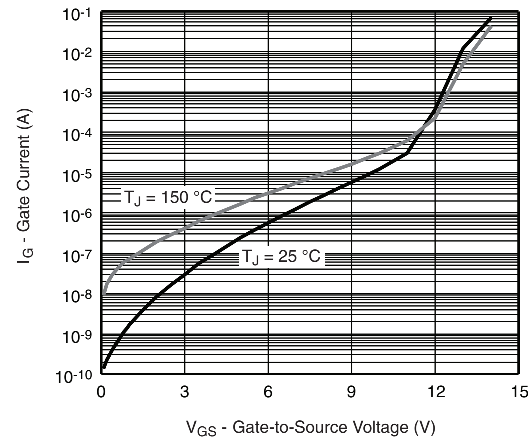
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

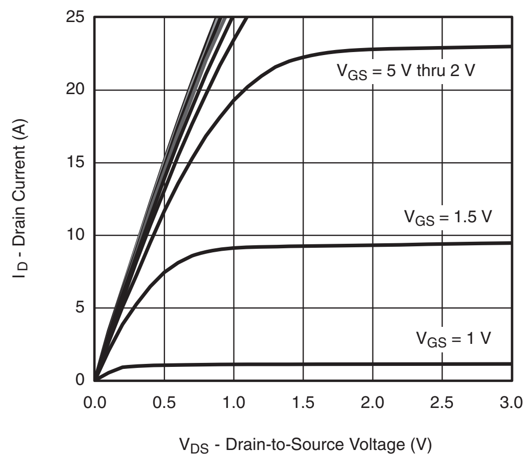
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



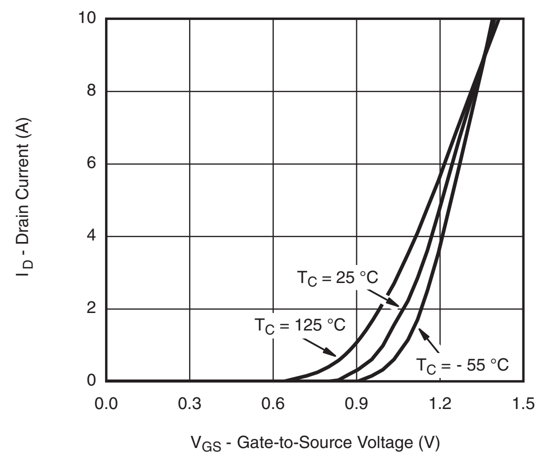
Gate Current vs. Gate-to-Source Voltage



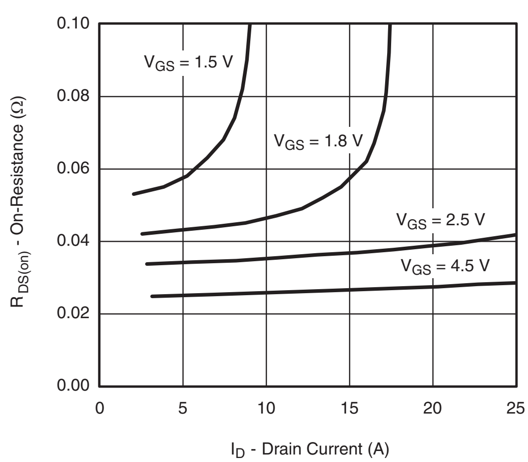
Gate Current vs. Gate-to-Source Voltage



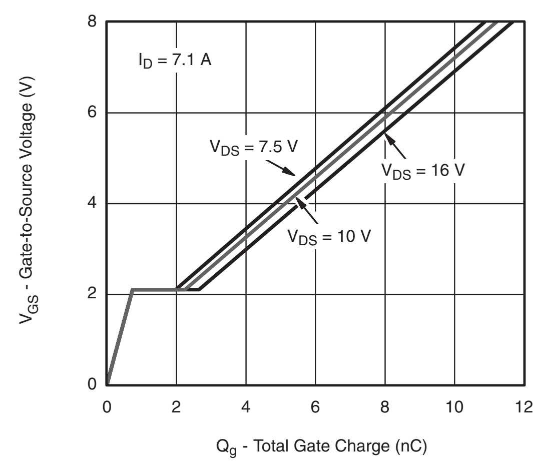
Output Characteristics



Transfer Characteristics

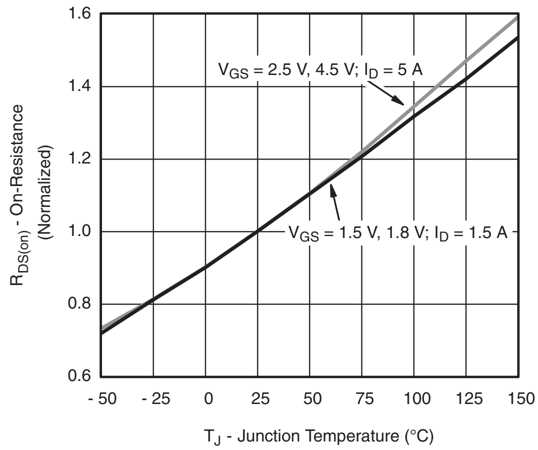


On-Resistance vs. Drain Current

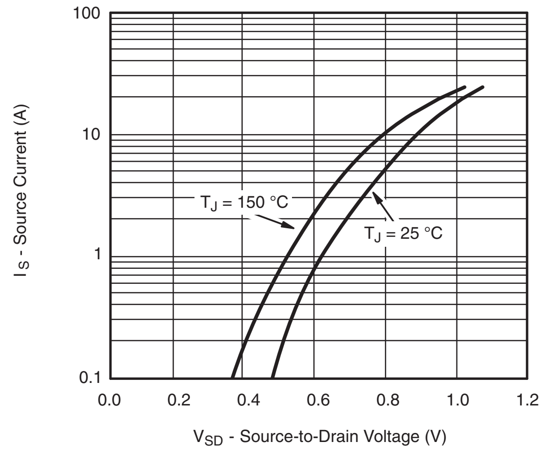


Gate Charge

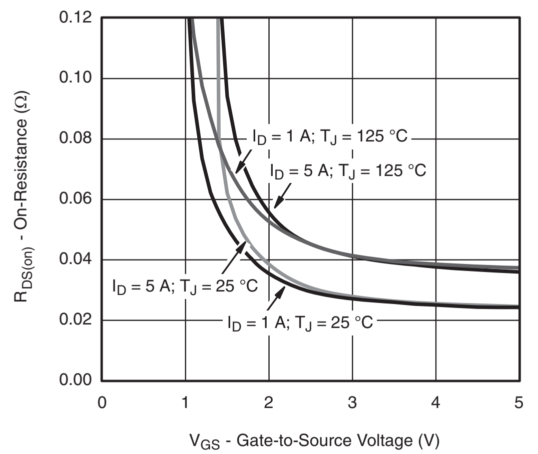
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



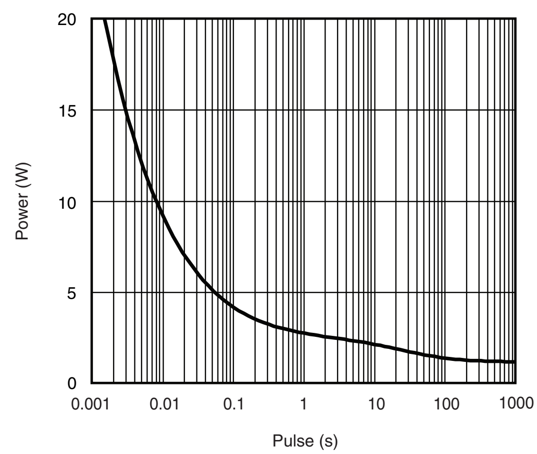
Normalized On-Resistance vs. Junction Temperature



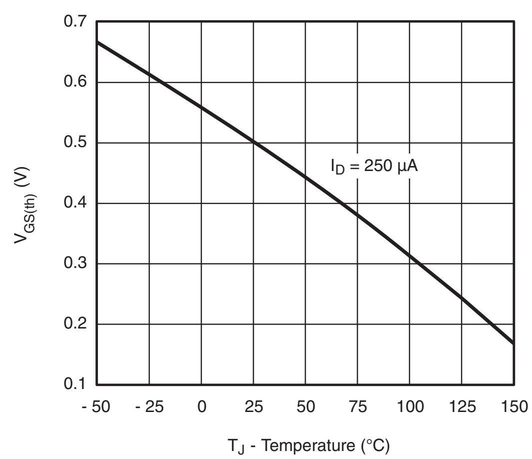
Source-Drain Diode Forward Voltage



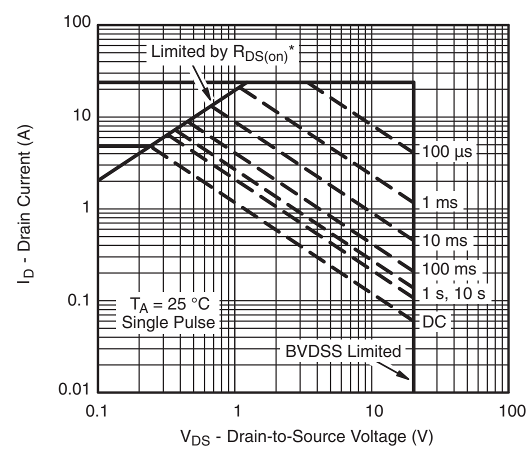
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



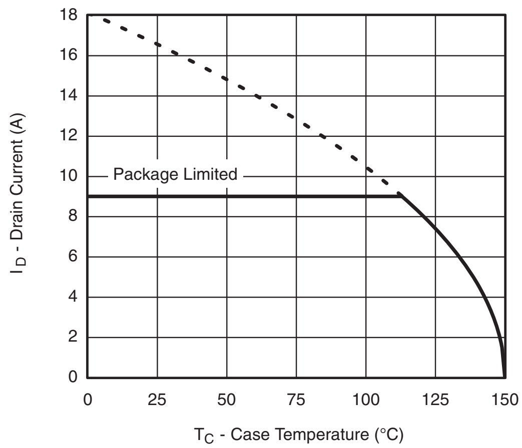
Threshold Voltage



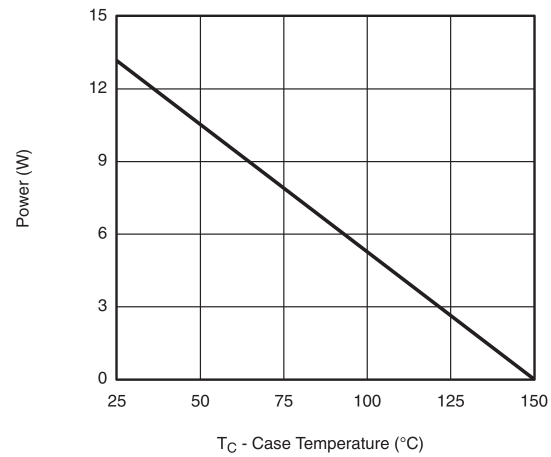
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Current Derating [a]

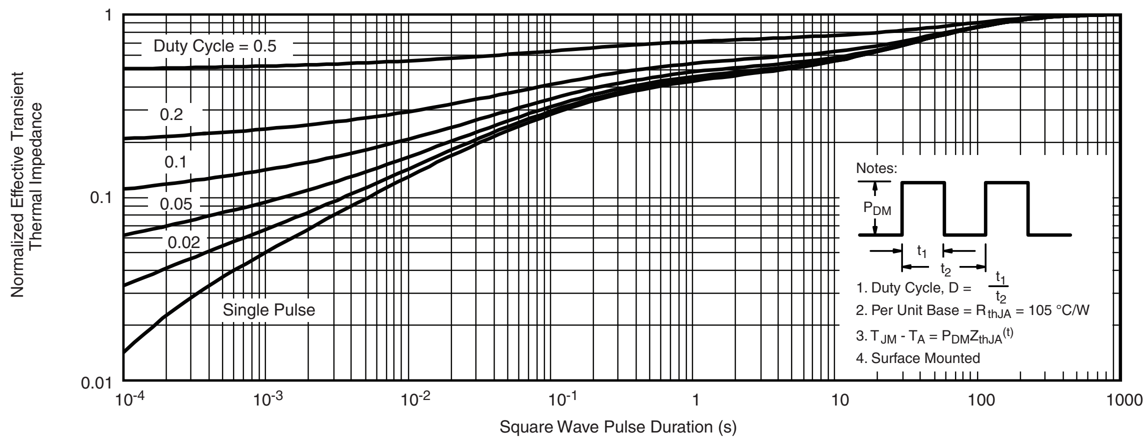


Power Derating

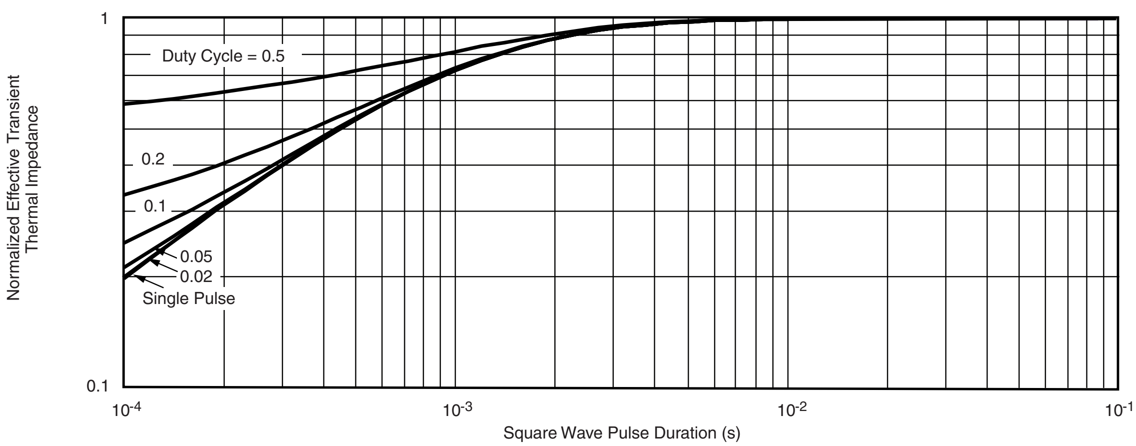
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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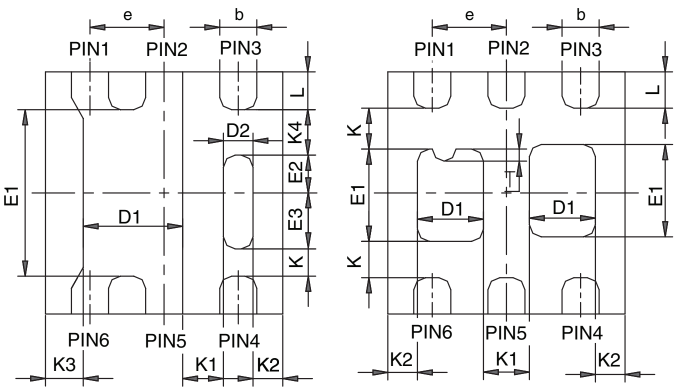
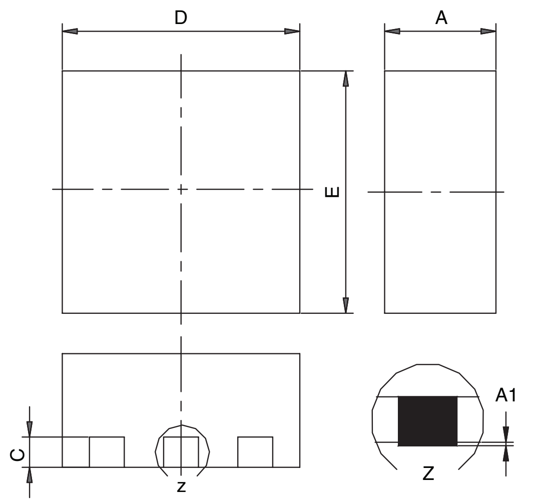
PowerPAK® SC75-6L



BACKSIDE VIEW OF SINGLE   BACKSIDE VIEW OF DUAL



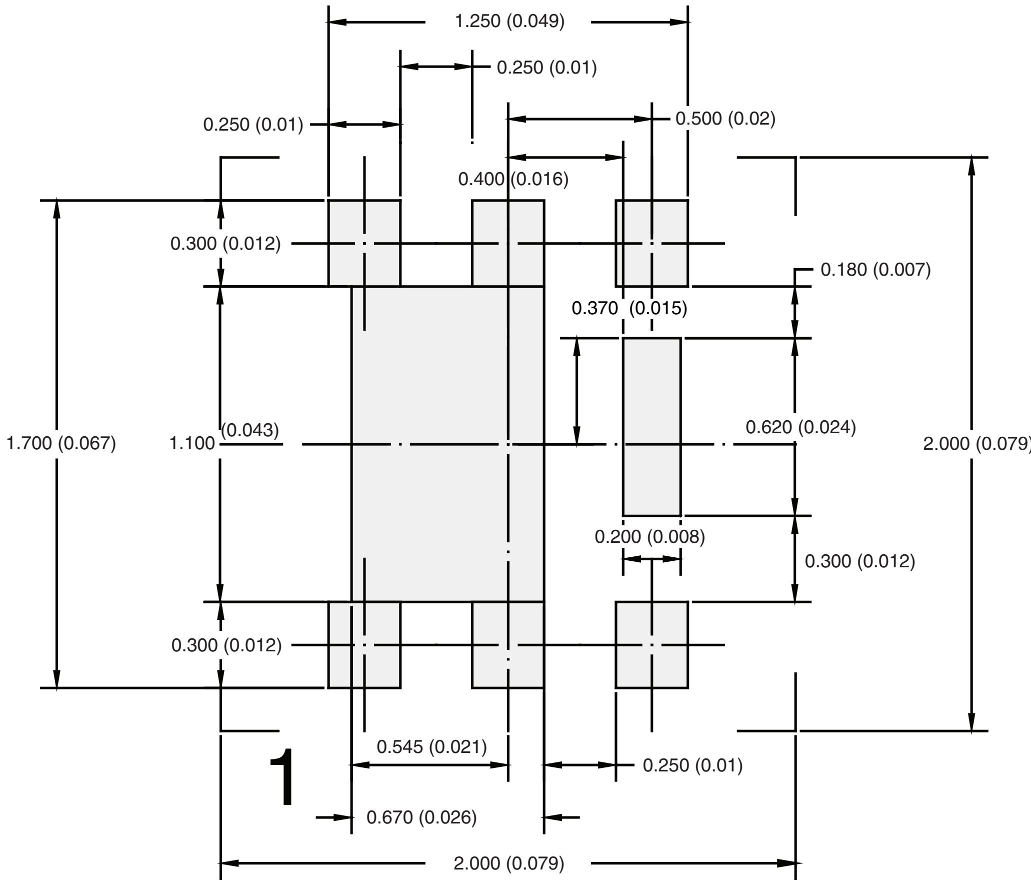
DETAIL Z

Notes:
1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5935

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Single



Dimensions in mm/(Inches)

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