AVS / DVS and Margining Circuits for Vishay Power ICs SiC40X Series SMPS Regulators

by Ronald Vinsant

ABSTRACT

There are many applications that require that a voltage rail within a system be capable of being adjusted by a digital or analog control signal. These circuits may only need to do a margining function in a test mode, vary the output voltage from the regulator by only a small amount to optimize specific performance parameters, or perhaps the voltage must be widely scalable to allow for the use of different sensors in an industrial application. This application note will show a number of different solutions to these design challenges by utilizing the Vishay SiC40X series of synchronous buck regulators. A key aspect of this design is the COT architecture of this family of products, which allows adaptability of the control system to the different operating points of the regulator without any iterative compensation design.

A spreadsheet tool and simulation schematic will be introduced that enable the user to quickly derive a solution with knowledge of only a few required parameters. Confirmation of the validity of these two tools will be shown by use of the SiC401DB, SiC402DB, and SiC403DB reference board, with the addition of only two resistors, a capacitor, and a user-supplied voltage source. This source could be an existing rail with an analog switch, a GPIO or PWM on an FPGA or processor, or a DAC.

SiC40X DESCRIPTION

The Vishay Siliconix SiC401A/B, SiC402A/B, and SiC403A/B are advanced stand-alone synchronous buck regulators, featuring integrated power MOSFETs, a bootstrap switch, and a programmable LDO in space-saving PowerPAK® MLP55-32L pin packages.

The SiC401A/B, SiC402A/B, and SiC403A/B are capable of operating with all ceramic solutions and switching frequencies up to 1 MHz. The programmable frequency, synchronous operation, and selectable power-save feature allow operation at high efficiency across the full range of load current. See www.vishay.com/doc?62768.

THE REFERENCE BOARD

This reference board allows the end user to evaluate the SiC401A/B, SiC402A/B, and SiC403A/B for their features and all functionalities. It can also be a reference design for a user's application. See www.vishay.com/doc?62923.

CALCULATION TOOLS

The designer can start their design by using the reference board mentioned above. If the reference board does not meet the goals of the designer's application, then a design tool is available online at www.vishay.com/doc?62923.

Once a regulator design has been chosen, there is an Excel tool, an AVS calculator, located at www.vishay.com/doc?77389.

This tool allows the designer to add to the existing regulator circuit adjustability of the output voltage through an external signal from a DAC or other voltage source. In addition, this spreadsheet has some programmer's tools to make the writing of software to drive the DAC easier.

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HOW IT WORKS

Theory

To describe the theory of operation, a design from Vishay's AVS calculator tool has been chosen that extends to the boundaries of operation of the SiC40X family of regulators (Fig. 1). The yellow cells indicate the only parameters required from a user to generate a design. Details of the calculator will be covered later in this application note.

Step 1:	Calculate R_{TOP} and R_{DAC}							
V_{REF} (V)	R_{BOT} (R23 above) (Ω)	I_{RBOT} (A)	SiC4XX V_{OUT} max. (V)	SiC4XX V_{OUT} min. (V)	Determine DAC gain (DAC V / output V) (ratio)	Determine zero R_{DAC} current point for V_{OUT} ($V_{DAC} = V_{REF}$) (V)	Calculate R_{TOP} (Ω)	Calculate R_{DAC} (Ω)
0.6	5110	0.000117	5	0.25	-1.9	3.86	27764.33	14612.81
Step 2:	Input DAC parameters							
DAC max. V_{OUT} (V)	DAC bits (number)	DAC LSB (V)	1 DAC LSB adjust in SiC4XX V_{OUT} (V)	Total count (theoretical number of voltage steps from DAC) (number)				
2.5	16	3.81^{-5}	7.24792^{-5}	65536				

Fig. 1 - Calculation Results for Theory of Operation

Fig. 2 shows a schematic of the reference board. The area circled in black is where a signal will be injected to alter the output voltage. R53, R54, and C38 have been added to the original schematic. In all the simulations below, the op-amps that are used are very close to ideal, thus the calculations are very exacting.

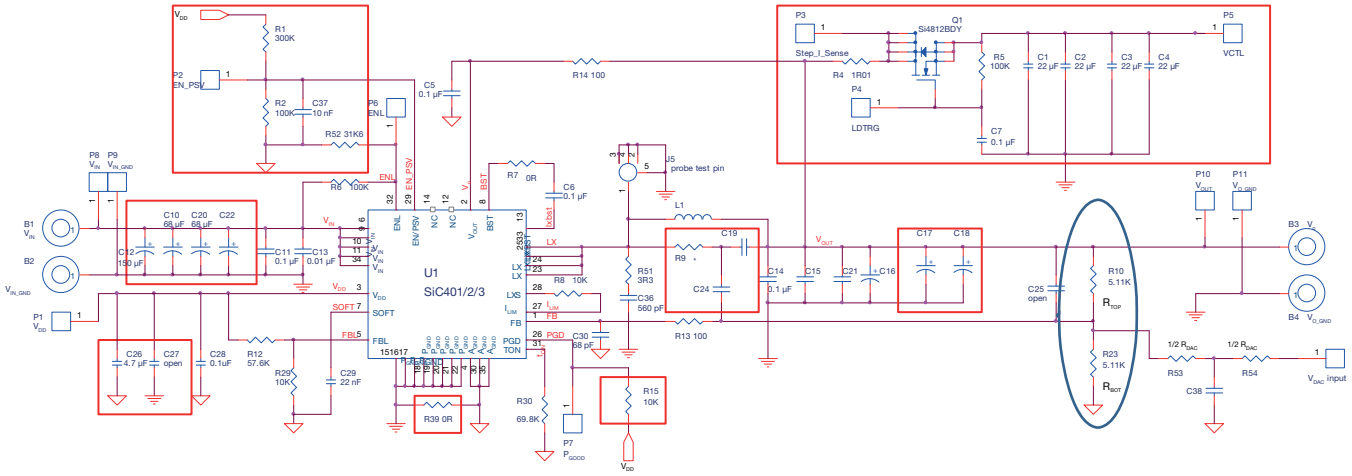

Fig. 2 - Reference Board Schematic (Modified)

The circled area in Fig. 2 provides a simplified view of DC operation.

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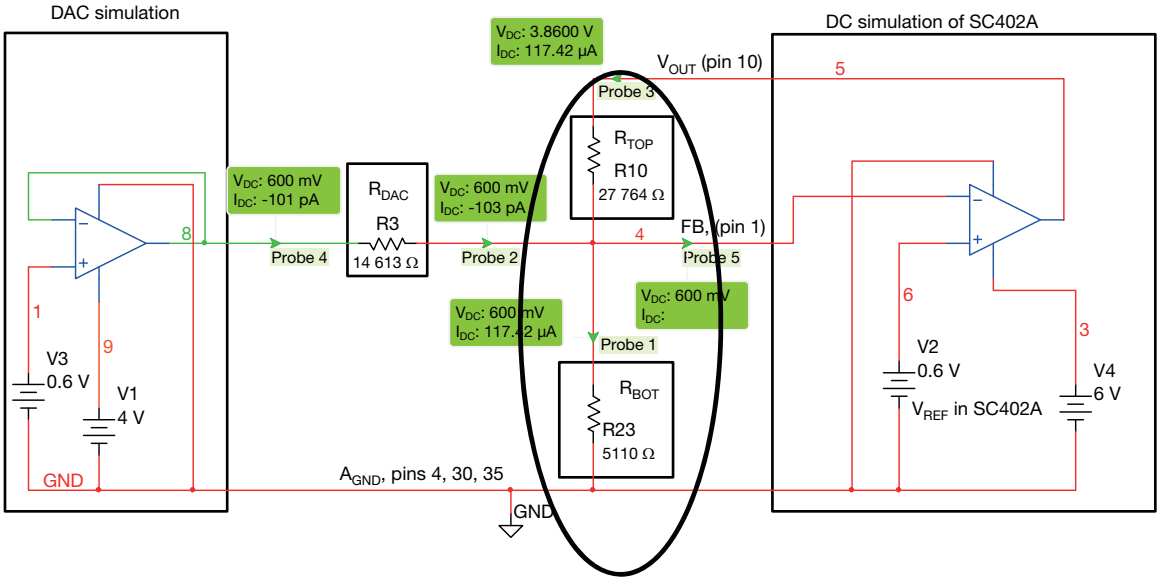

Fig. 3 - Operation at "Zero R_{DAC} Current Point"

In Fig. 3 it can be observed that the SiC40X control loop will maintain the reference voltage, V2, at "FB, pin 1" under normal operation. It can be assumed then that the current in R23, R_{BOT}, will always be 117 µA. It can be further observed using Kirchhoff's Current Law that the sum of the currents at node 4 from R_{DAC} and R_{TOP} must be equal to the current in R_{BOT}. The case shown in Fig. 3 is the "zero R_{DAC} current point" from the calculator in Fig. 1, where the voltage at probe 4, node 8 is equal to the voltage at probe 2, node 4. At this operating point, all current to R_{BOT} has to be supplied by R_{TOP}. The DAC has no effect on V_{OUT}. Thus: $V_{OUT} = 0.6 \times (1 + R10/R23) + V_{RIPPLE}/2$ (see SiC40X datasheets for further information).

Now let's examine lowering the voltage at probe 4, V_{DAC}.

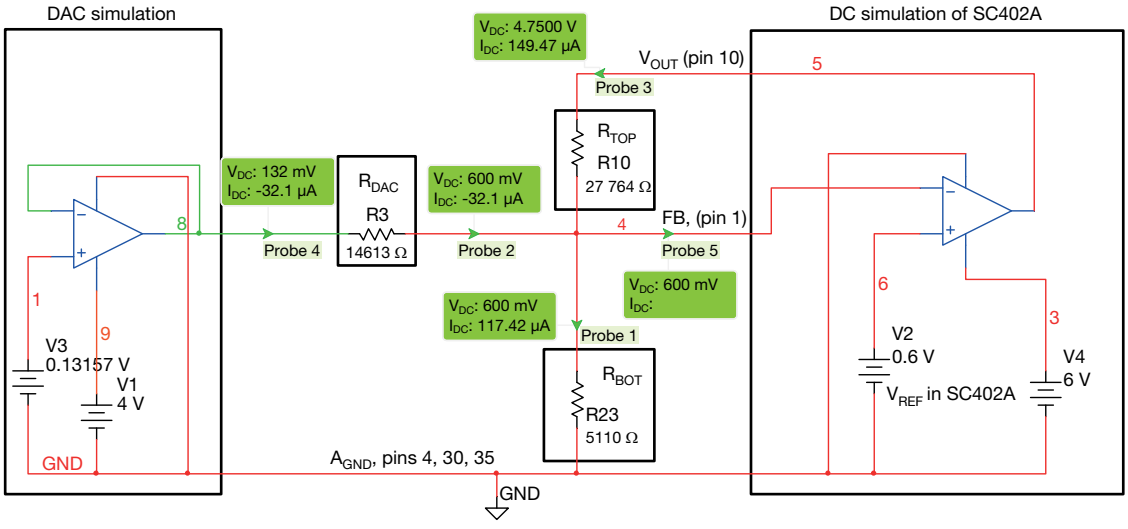

Fig. 4 - Operation at V_{DAC} Lower than V_{REF}

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As the DAC voltage is changed below the reference voltage (V_{REF} at node 6 in Fig. 4), the current through R_{DAC}, R3, goes negative. To make up for current being drawn out of node 4, the output voltage has had to rise so that there is more current from R_{TOP} to make up for the current drawn out through R_{DAC}, as can be observed in probes 2, 4, and 3. Notice that the voltage across R_{BOT}, R23, is still 0.6 V, thus the current in R23 is constant at 117 µA.

The next step is to raise the voltage at probe 4, V_{DAC}.

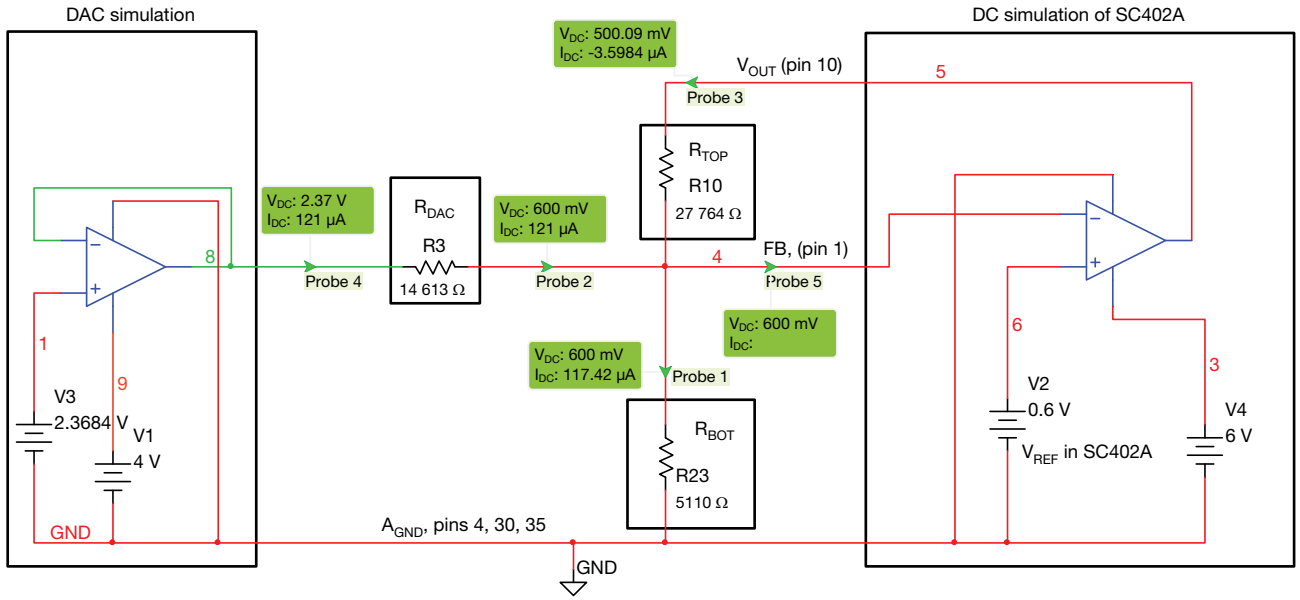

Fig. 5 - Operation at V_{DAC} Higher than V_{REF}

Fig. 5 simulates a rise in the DAC voltage above V_{REF}, node 6, and the current through R_{DAC}, R3, has gone positive. To make up for this current being forced into node 4, the output voltage has had to fall so that current has to be pulled out of node 4 through R_{TOP} to make up for the current being sourced through R_{DAC}, as can be observed in probes 2, 3, and 4. Notice that the voltage across R_{BOT}, R23, is still 0.6 V, thus the current is constant at 117 µA. In this case V_{OUT} from the SiC40X is actually below V_{REF}, V2.

CONTROL LIMITS OF V_{OUT}

There is a sacrifice in performance that is made though when V_{OUT} goes too far below V_{REF} and the current from R_{DAC} becomes positive; as this current forces V_{OUT} lower, the effective open loop gain of the regulator declines. Put simply, the output voltage regulation gets worse. This is due to the inability of the SiC40X control system to work close to a zero duty cycle and its circuitry to operate near to or at zero volts.

The values shown in the circuit in Fig. 5 were used in the reference board in Fig. 2, which was constructed and tested for output voltage regulation at three operating points: 5 V (Fig. 6), 0.25 V, and the "zero R_{DAC} current point" of 3.9 V with a fixed 12 V input to demonstrate this point.

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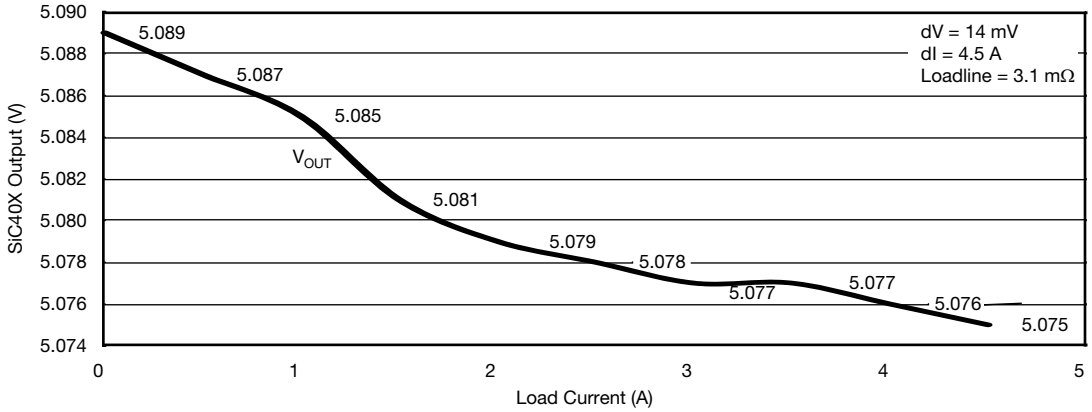

Fig. 6 - 5 V Output Load Regulation

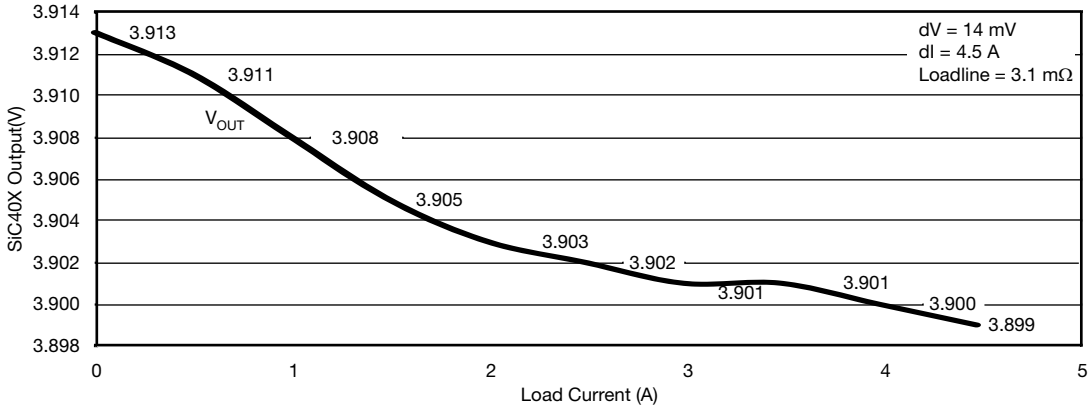

Fig. 7 - 3.9 V Output Load Regulation

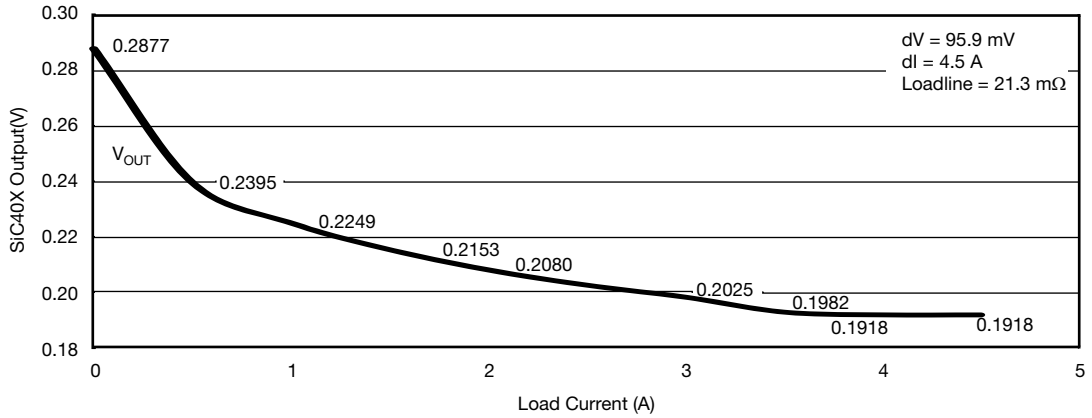

Fig. 8 - 0.25 V Output Load Regulation

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There is no difference in the regulation of the 5 V and 3.9 V outputs, but the 0.25 V output regulation is substantially worse, as expected. Practical limits for wide output range designs are from 1.5 V to 5 V for reasonable output regulation. See circuit 3 as an example.

Key point: Optimal performance occurs with V_{OUT} at levels from 1.5 V to 5 V.

ADDITIONAL DESIGN CONSIDERATIONS

Besides the obvious error terms of resistor and V_{REF} tolerance (see "How to Obtain Exacting Resistor Values"), there are a number of other issues that can affect the output voltage tolerance. Let's look at the boundary conditions of the control system.

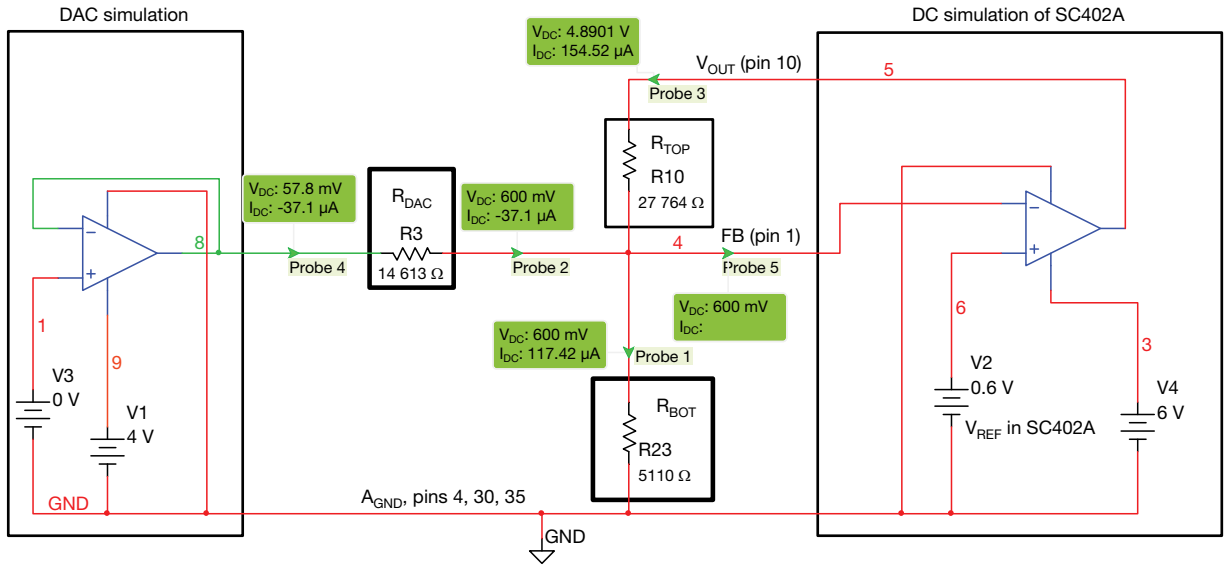

Fig. 9 - DAC Limitation at Zero Volt Output

If V_{DAC} is brought to zero volts, as in Fig. 9, V_{DAC}, probe 4 is at 57.8 mV, not zero. That is due to the inability of most DACs to actually get to zero volts, even "rail-to-rail" designs.

Key point: these designs are based on an "ideal" voltage source.

Allowances may need to be made for deviations from the ideal.

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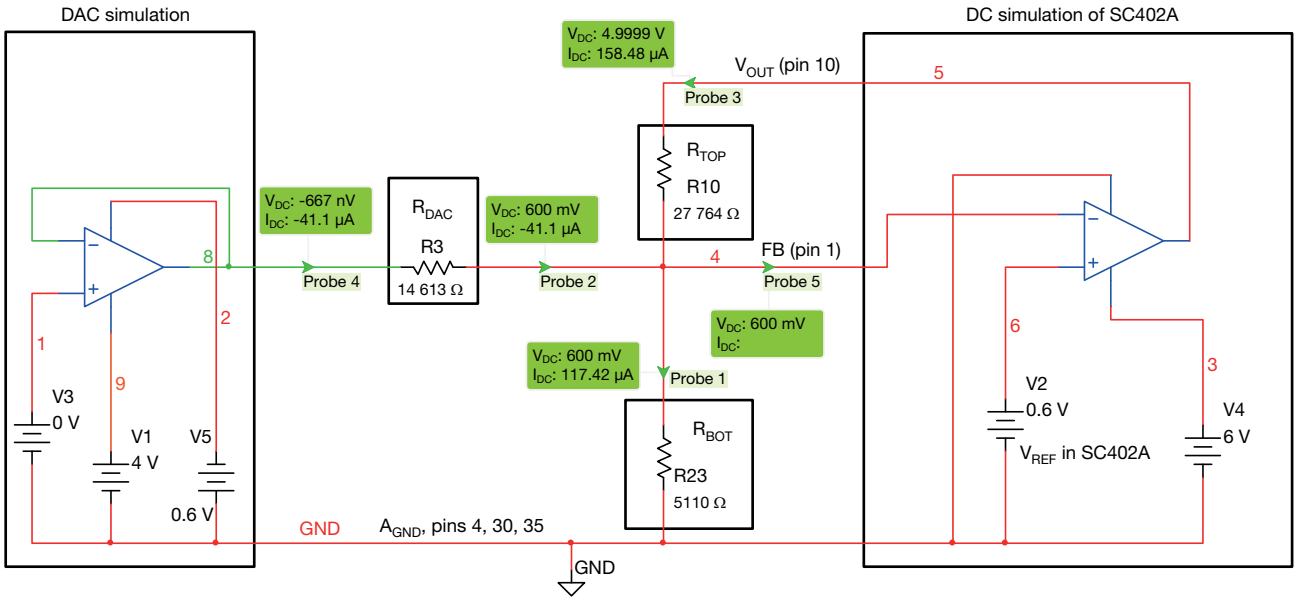

Fig. 10 - Addition of Negative Rail to DAC Buffer

In Fig. 10 a negative voltage, V5, is added to the DAC circuit and now the output of the DAC simulation at node 8 actually goes to zero volts and the regulator output voltage matches that of the calculator spreadsheet. A DAC with a buffer can have a negative supply to allow V_{DAC} to go to zero.

Key point: watch for non-linearity in the DAC (voltage source), both at the lower and upper ends of its output range.

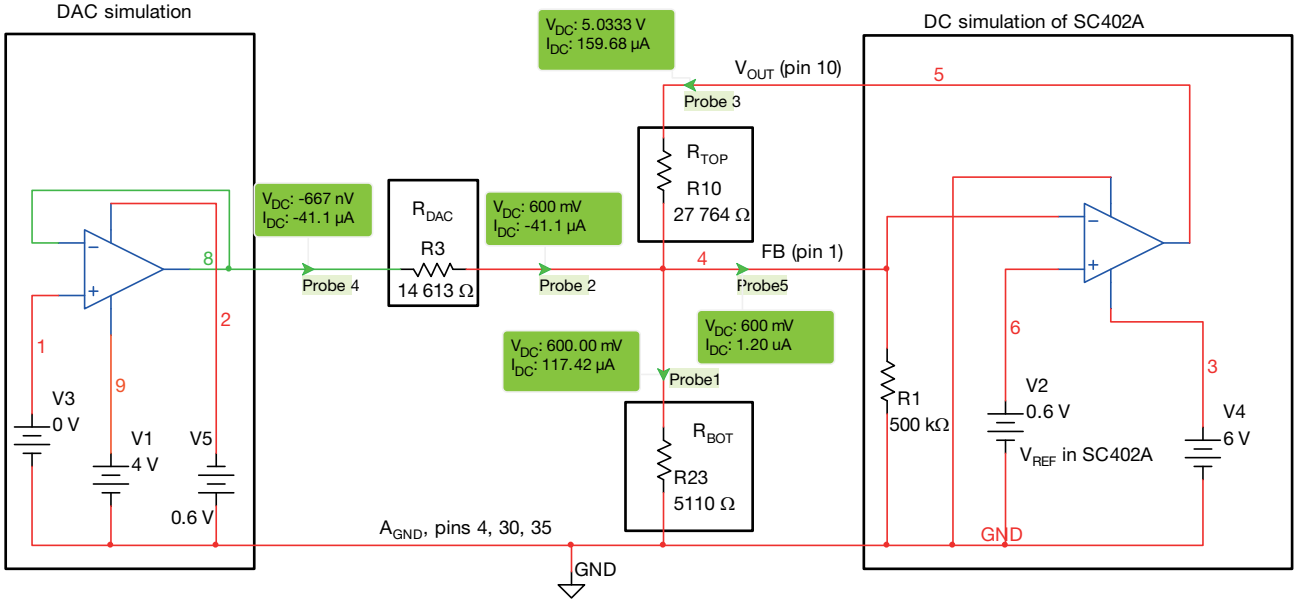

Fig. 11 - Simulation Showing Effect of Input Bias Currents

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If there is an input current required on the "FB, (pin 1)," then this current will subtract from R_{BOT}, R23. In the simulation in Fig. 11, R1, a 500 kΩ resistor, was added from "FB, (pin 1)" to ground. This requires that an additional 1.2 µA be supplied by R_{TOP} so the output voltage, observed at probe 3, rises by 33 mV to add the required current to keep node 4 at 0.6 V.

Key point: watch for input offset currents.

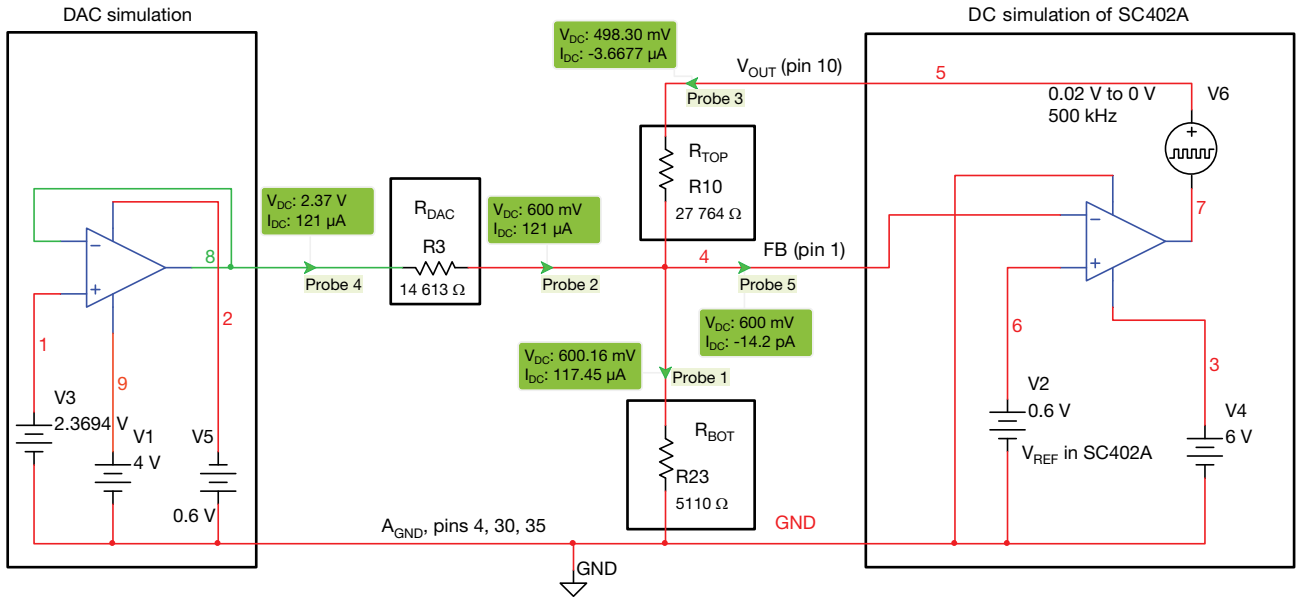

Fig. 12 - Effect on V_{OUT} Setting Due to Influence of Ripple

Referring to Fig. 12, let us look at the effects of ripple on V_{OUT}. Since most switching regulators have some output ripple, one has to consider that this is a noise component whose average value can affect the feedback of the regulator.

Referring back to Fig. 5, it can be seen that when we set the DAC voltage in our simulation of this design to 2.3684 V (shown as 2.37 V at probe 4), we get an output of 500.09 mV.

If we then add a 20 mV peak-to-peak 500 kHz "ripple" to the output and R1 (as shown in Fig. 11) is removed so that the offset current will not influence the result, we can observe the effect of the injected ripple signal.

The output voltage has dropped about 2 mV, demonstrating that ripple and noise can affect V_{OUT} also. In an actual application where the bandwidth of the control loop is less than the op-amps in the simulation model, the effect will be greater; typical values are 5 mV to 10 mV.

CALCULATOR

The calculator requires that users know five different parameters:

1. V_{REF}
2. R_{BOT}
3. SiC40X output voltage range (the minimum voltage and the maximum voltage)
4. The maximum output voltage of the DAC
5. The number of DAC bits

All other parameters are calculated for users.

There is a section that is useful for programmers that allows the translation of DAC counts in decimal and hex format to V_{OUT} and V_{DAC}.

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EXAMPLE DESIGNS

Circuit 1: AVS Design

This is a circuit that would be useful to most AVS and margining applications that are in the 1 V region. Fig. 13 shows the results from the spreadsheet design tool.

Step1:	Calculate R_{TOP} and R_{DAC}								
V_{REF} (V)	R_{BOT} (R23 above) (Ω)	I_{RBOT} (A)	SiC4XX V_{OUT} max. (V)	SiC4XX V_{OUT} min. (V)	Determine DAC gain (DAC V / output V) (ratio)	Determine zero R_{DAC} current point for V_{OUT} ($V_{DAC} = V_{REF}$) (V)	Calculated R_{TOP} (Ω)	Calculated R_{DAC} (Ω)	$R_{DAC}/2$ (Ω)
2.5	5110	0.000489237	3.4	3.1	-0.12	3.1	1226.4	10 220	5110
Step 2:	Input DAC or voltage source parameters								
DAC max. V_{OUT} (V)	DAC bits (number)	DAC LSB (V)	1 DAC LSB adjust in SiC4XX V_{OUT} (V)	Total count (theoretical number of voltage steps) (number)					
2.5	12	0.000610352	7.32422^{-5}	4096					

Fig. 13 - Design Tool Calculations for Circuit 1

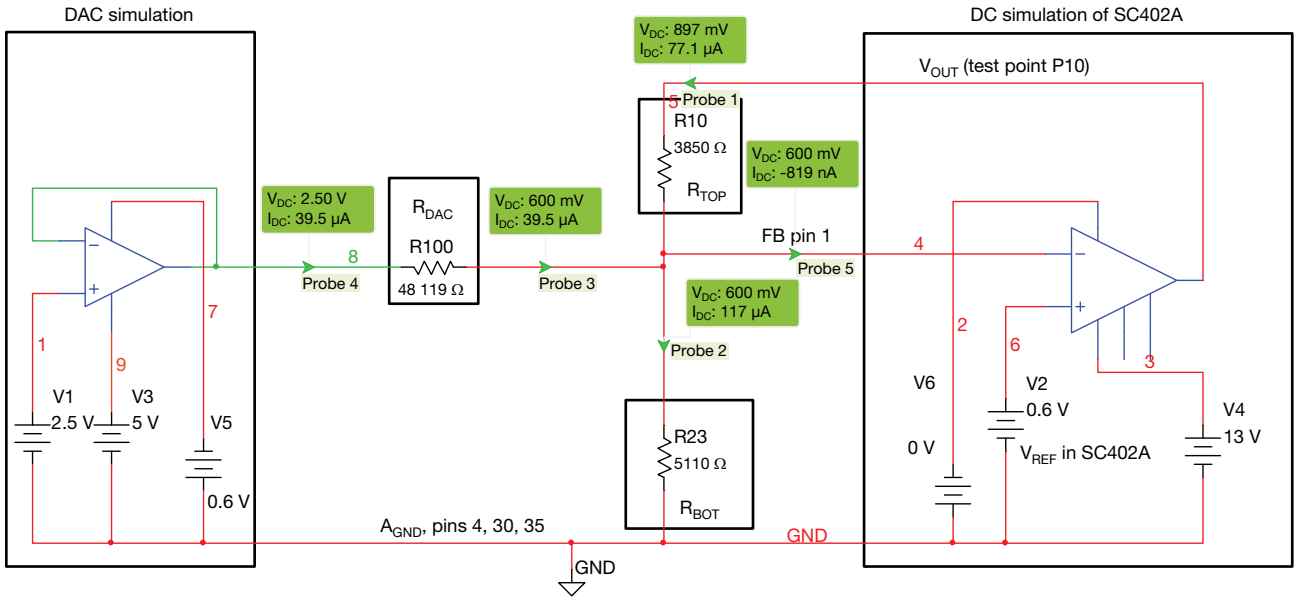

Fig. 14 - Simulation Schematic (Refer to Fig. 2 for Actual Schematic)

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Shaping V_{OUT} Response

Fig. 2 shows how R_{DAC} has been cut in half so that there are two resistors, R53 and R54, allowing a capacitor to be added in between them. This capacitor will shape the response of V_{OUT} to a transition command from the V_{DAC}.

If the response time, t_r, is set at five time constants so it is close to 20 µs, this will result in the best response time of the regulator. This time can be determined from:

$t_r = 1/(f_{sw} \times 0.1)$ and $t_r = (R_{total}) \times C38 \times 5$,

where: $R_{total} = R54 \parallel R53$ for $f_{sw} = 500$ kHz, then:

$1/(0.1 \times 500\,000) = 20 \times 10^{-6}$ s, or 20 µs. Divide by five and something close to 5 µs is required.

Since R54 has been set equal to R53, then $R54 \parallel R53 = 0.5 \times R53$ or 12 kΩ. Thus:

12 kΩ x 470 pF = 5.64 µs x 5 is 28.2 µs. 470 pF was chosen as it is a standard value.

In a simulator it looks like this, where the reference values (R54, C38, and R53) refer to Fig. 2:

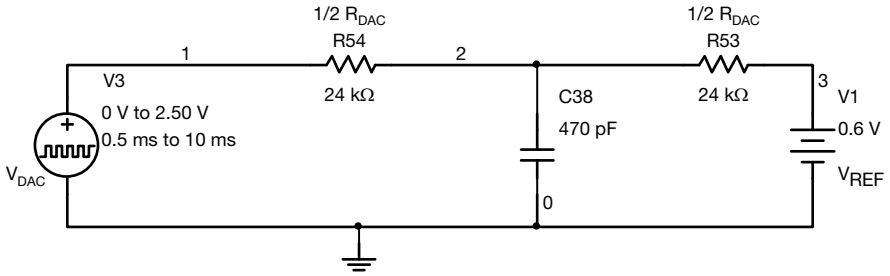

Fig. 15 - Transient Simulation Circuit

These are the simulation results.

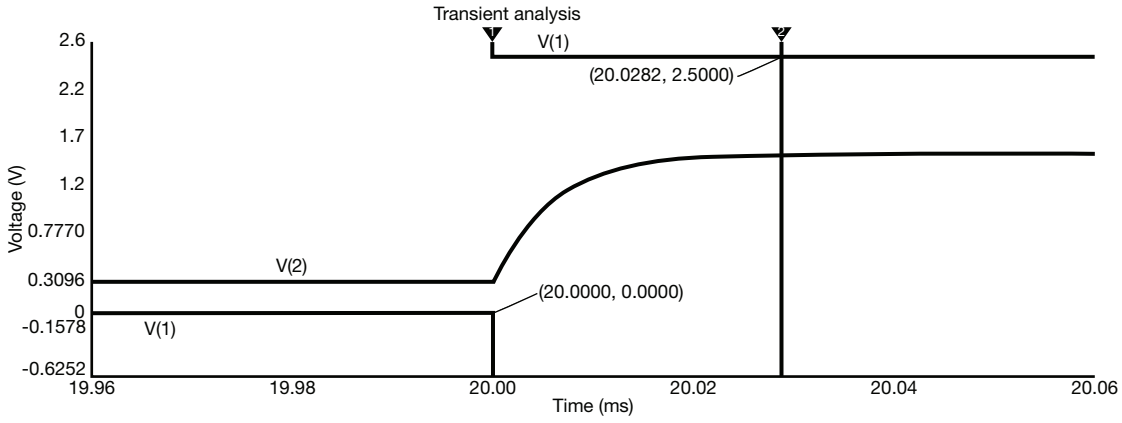

Fig. 16 - Transient Step Simulation Result
(Note: V1 and V2 Refer to the Voltages at the Nodes 1 and 2, not to the Sources V1 and V2)

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Here is what the output voltage transition of the regulator looks like (showing a 10 % to 90 % rise time):

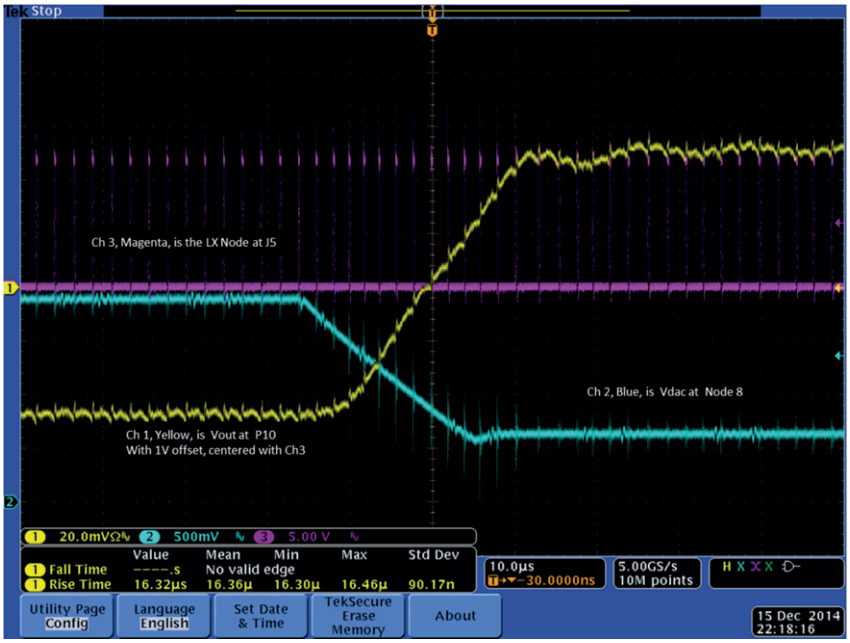

Fig. 17 - V_{OUT} Transition at no Load

Referring to Fig. 2, channel 1 is a regulator V_{OUT} at P10 (yellow) with 1 V offset, channel 2 is V_{DAC}, and channel 3 is the LX node at J5. Conditions are no load on V_{OUT}, 12 V input.

Here is the same transition but with a 6 A load (all scope settings the same as Fig. 17):

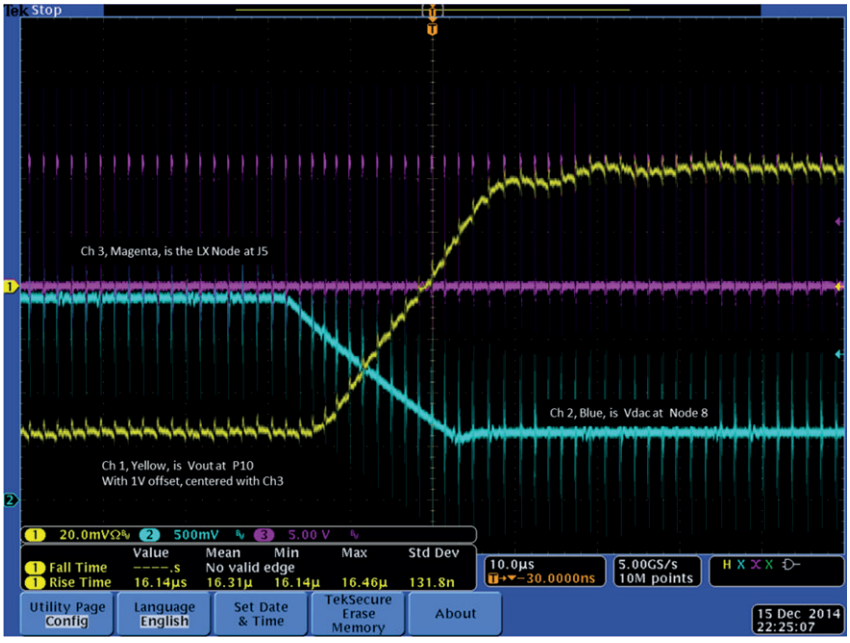

Fig. 18 - V_{OUT} Transition at 6 A Load

Key point: loading does not substantially affect the V_{OUT} transition speed.

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Transient Response of Circuit 1

Again, referring to Fig. 2, let us look at how the COT architecture of the SiC40X results in a fast response to both load and V_{DAC} commands.

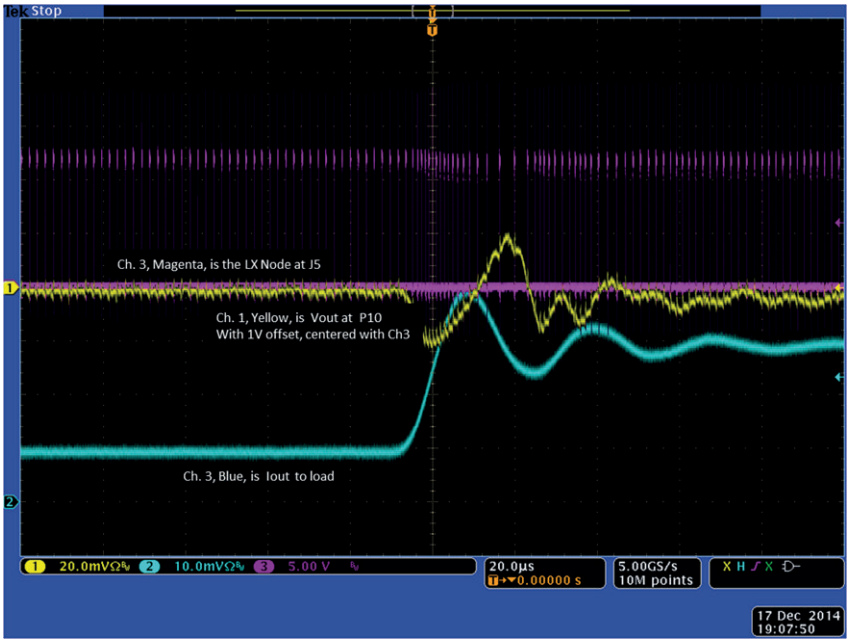

Fig. 19 - Increasing Transient Load with Static DAC Setting

Fig. 20 - Load Release with Static DAC Setting

Whenever two parameters change at one time, there might be unwanted effects. Let us look at what happens when both V_{OUT} and load current are changed together.

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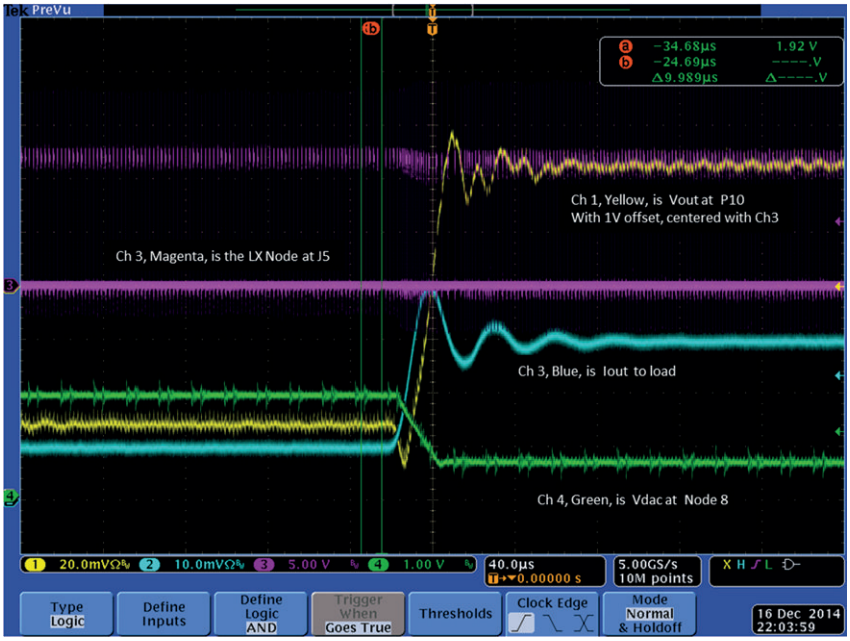

Fig. 21 - Increasing Load from 2 A to 6 A, V_{OUT} Increase from 0.95 V to 1.05 V Driven by a DAC

Let us examine the extremes; where V_{DAC} is driven from a function generator so that the V_{DAC} transition is 30 ns.

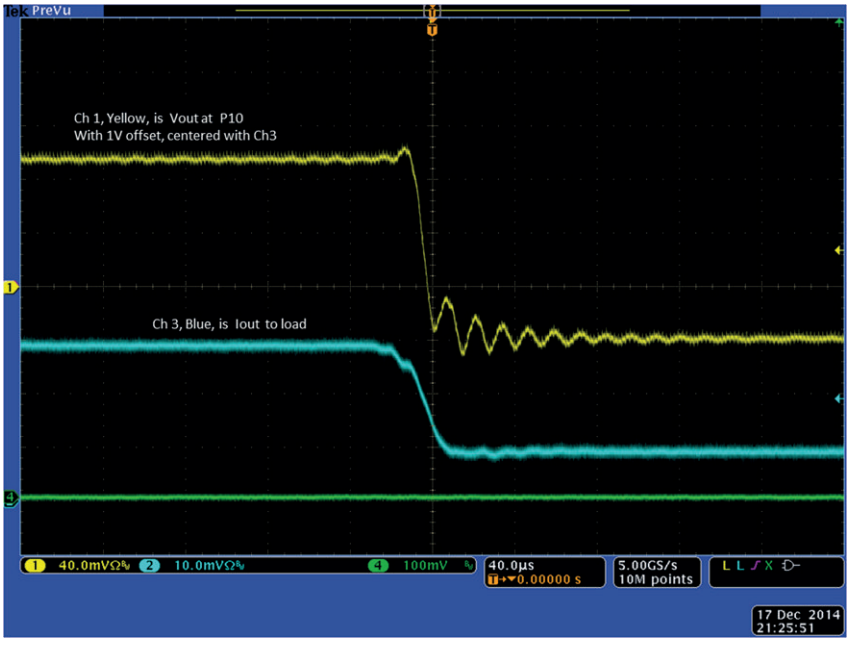

Fig. 22 - I_{OUT} Changes from 6 A to 2 A while V_{OUT} is Adjusted from 1.1 V to 0.96 V

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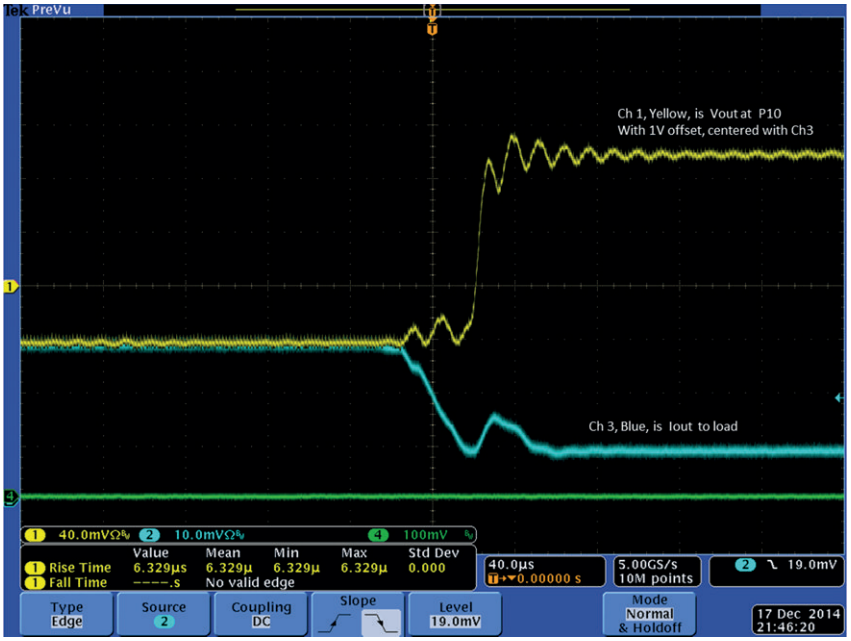

Fig. 23 - I_{OUT} Changes from 6 A to 2 A while V_{OUT} is Adjusted from 0.96 V to 1.1 V

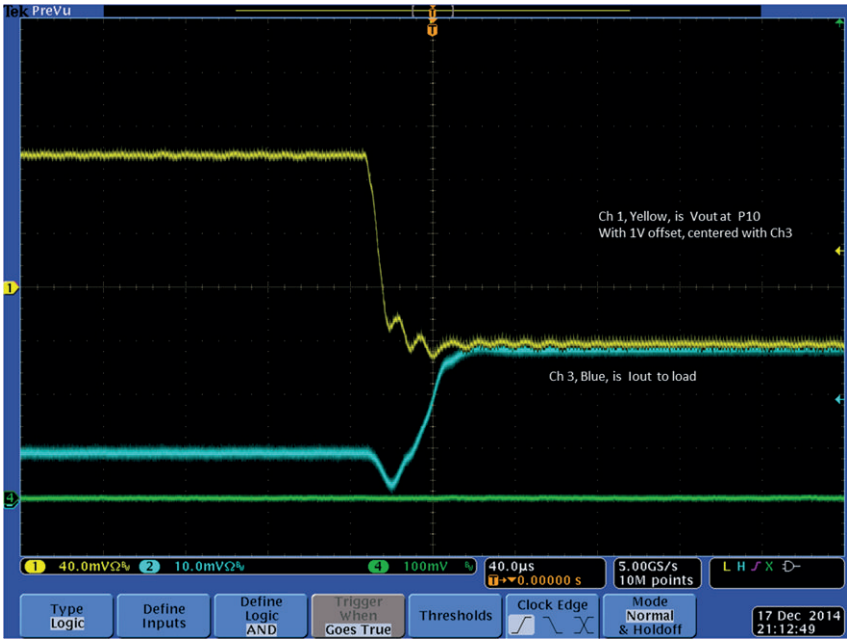

Fig. 24 - I_{OUT} Changes from 2 A to 6 A while V_{OUT} is Adjusted from 1.1 V to 0.96 V

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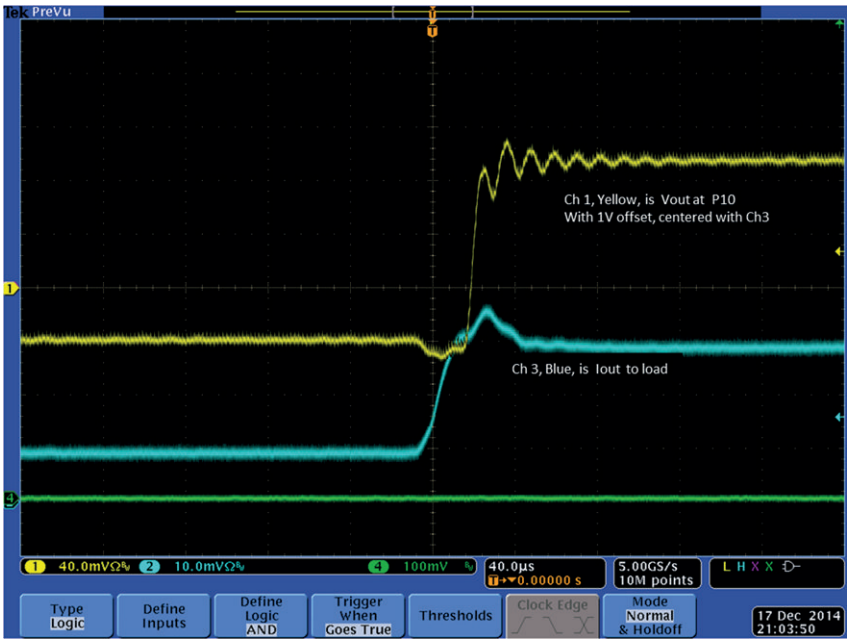

Fig. 25 - I_{OUT} Changes from 2 A to 6 A while V_{OUT} is Adjusted from 0.96 V to 1.10 V

Excellent transient performance is observed even under the worst case conditions due to the COT architecture of the SiC403A.

DC Load Regulation of Circuit 1

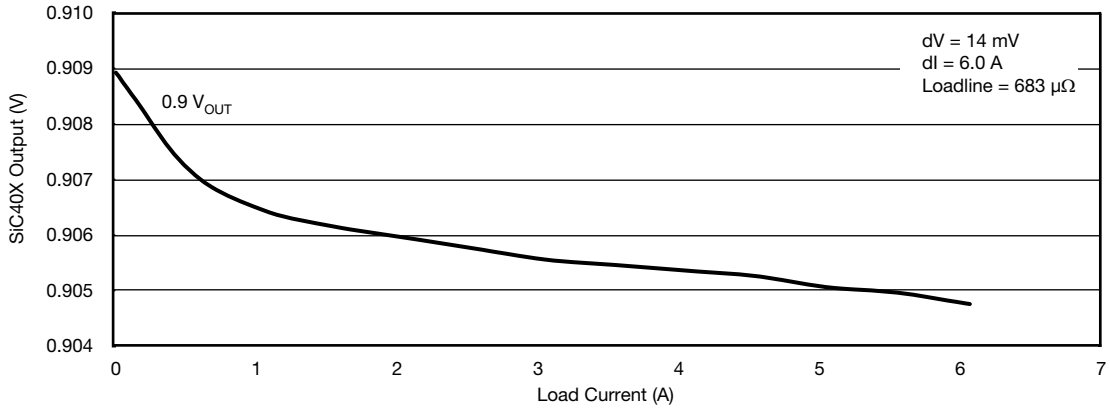

Fig. 26 - 0.9 V Load Regulation

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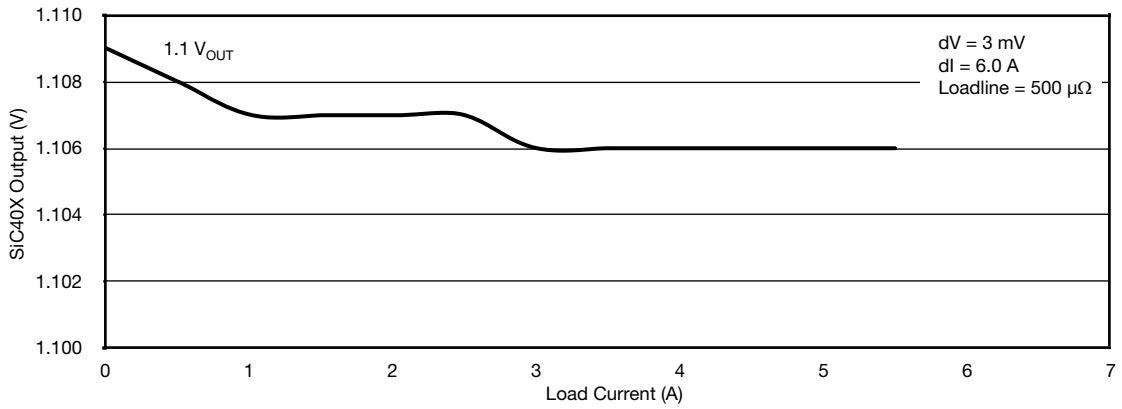

Fig. 27 - 1.1 V Load Regulation

Circuit 2: Using a Tri-State Buffer for a Voltage Margining Circuit

With a slight modification to circuit 1, a tri-state buffer can be used in place of the DAC as a three-output voltage source; V_{OUT} is selected by the state of the buffer. For purposes of the calculator, the buffer is a "0" bit DAC.

Step 1:	Calculate R_{TOP} and R_{DAC}								
V_{REF} (V)	R_{BOT} (R23 above) (Ω)	I_{RBOT} (A)	SiC4XX V_{OUT} max. (V)	SiC4XX V_{OUT} min. (V)	Determine DAC gain (DAC V / output V) (ratio)	Determine zero R_{DAC} current point for V_{OUT} ($V_{DAC} = V_{REF}$) (V)	Calculated R_{TOP} (Ω)	Calculated R_{DAC} (Ω)	R_{DAC} /2 (Ω)
0.6	5110	0.000117	1.1	0.9	-0.1111111	1.03333333	3691	33 215	16 608
Step 2:	Input DAC or voltage source parameters								
DAC max. V_{OUT} (V)	DAC bits (number)	DAC LSB (V)	1 DAC LSB adjust in SiC4XX V_{OUT} (V)	Total count (theoretical number of voltage steps) (number)					
1.8	0	1.8	0.2	1					

Fig. 28 - Tri-State Voltage Margining Circuit Calculation Result

If the buffer's output is active and is set to logic low, then there will be a 1.1 V output. If it is set at logic high, there will be a 1.1 V output. If at tri-state (not active), the V_{OUT} will be at the "zero R_{DAC} current point," or 1.03 V output. Any tri-state output could be used from an ASIC, FPGA, etc.

APPLICATION NOTE

AVS / DVS and Margining Circuits for Vishay Power ICs SiC40X Series SMPS Regulators

Here are the simulations:

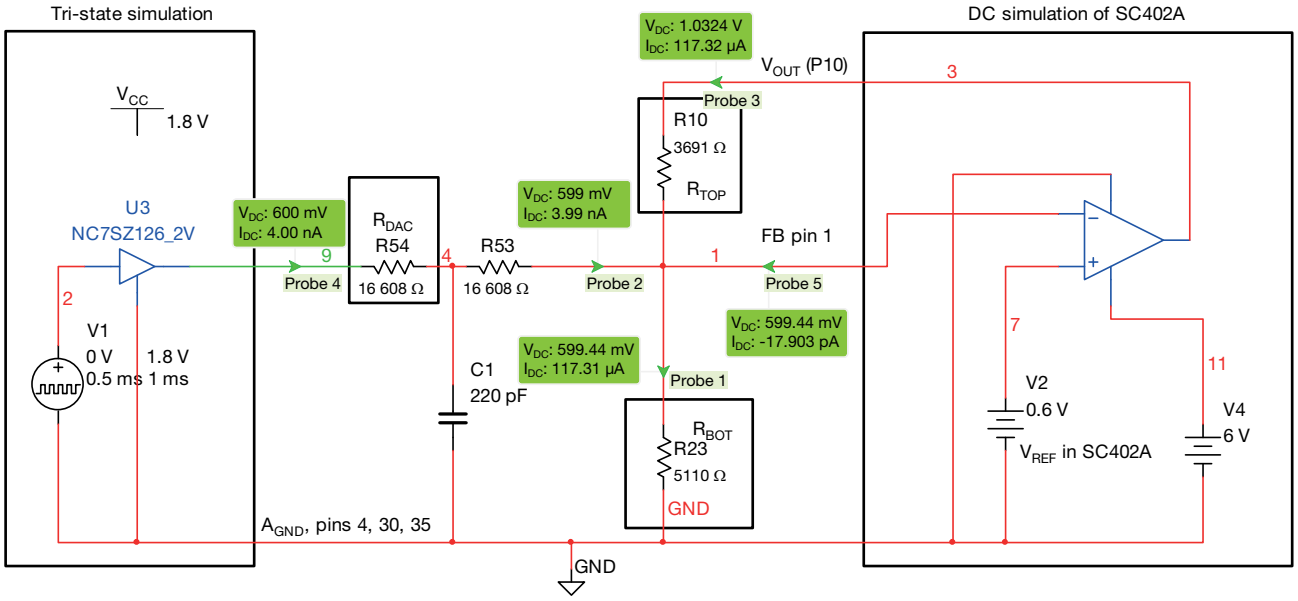

Fig. 29 - Tri-State Example with U3 at Tri-State

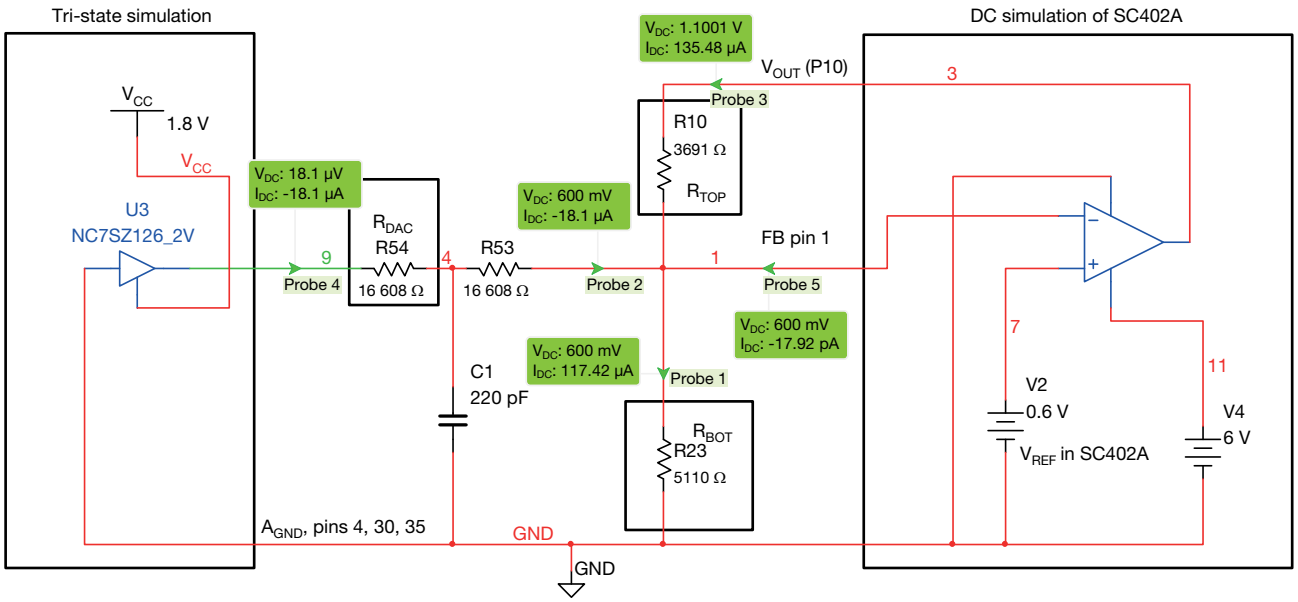

Fig. 30 - Tri-State Example with Tri-State not Active and Logic Output at Zero Volts

APPLICATION NOTE

AVS / DVS and Margining Circuits for Vishay Power ICs SiC40X Series SMPS Regulators

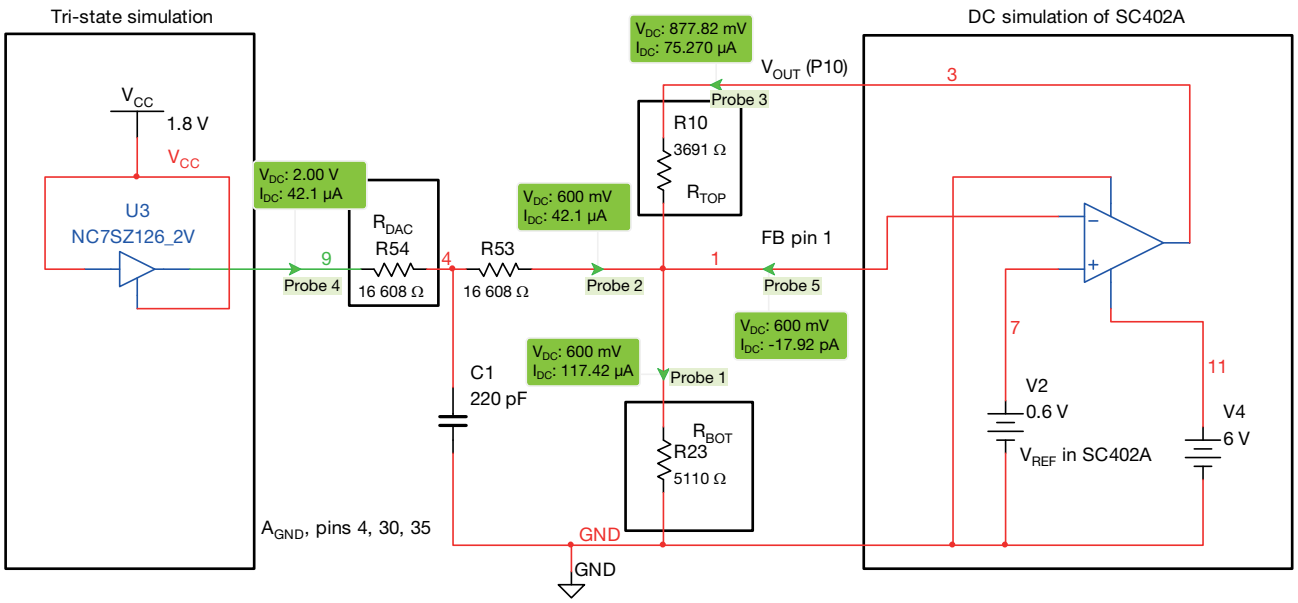

Fig. 31 - Tri-State Example with Tri-State not Active and Logic Output at 2 V

In Fig. 31 the simulation shows a V_{OUT} of 0.877 V rather than the 0.9 V designed for. This is due to an artifact of the simulation, as the model for the buffer assumes a 2 V power rail as opposed to the intended 1.8 V rail.

Circuit 3: Wide Range Output

This is a wide range output example. It would be useful for a designer that needs to set the rail for output buffers at different voltages such as 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V.

Step 1:	Calculate R_{TOP} and R_{DAC}								
V_{REF} (V)	R_{BOT} (R23 above) (Ω)	I_{RBOT} (A)	SiC4XX V_{OUT} max. (V)	SiC4XX V_{OUT} min. (V)	Determine DAC gain (DAC V / output V) (ratio)	Determine zero R_{DAC} current point for V_{OUT} ($V_{DAC} = V_{REF}$) (V)	Calculated R_{TOP} (Ω)	Calculated R_{DAC} (Ω)	$R_{DAC}/2$ (Ω)
0.6	5110	0.000117	5.25	1.45	-1.52	4.338	31835	20944	10472
Step 2:	Input DAC or voltage source parameters								
DAC max. V_{OUT} (V)	DAC bits (number)	DAC LSB (V)	1 DAC LSB adjust in SiC4XX V_{OUT} (V)	Total count (theoretical number of voltage steps from DAC) (number)					
2.5	10	0.002441	0.003710938	1024					

Fig. 32 - Circuit 3 Calculator Result

APPLICATION NOTE

AVS / DVS and Margining Circuits for Vishay Power ICs SiC40X Series SMPS Regulators

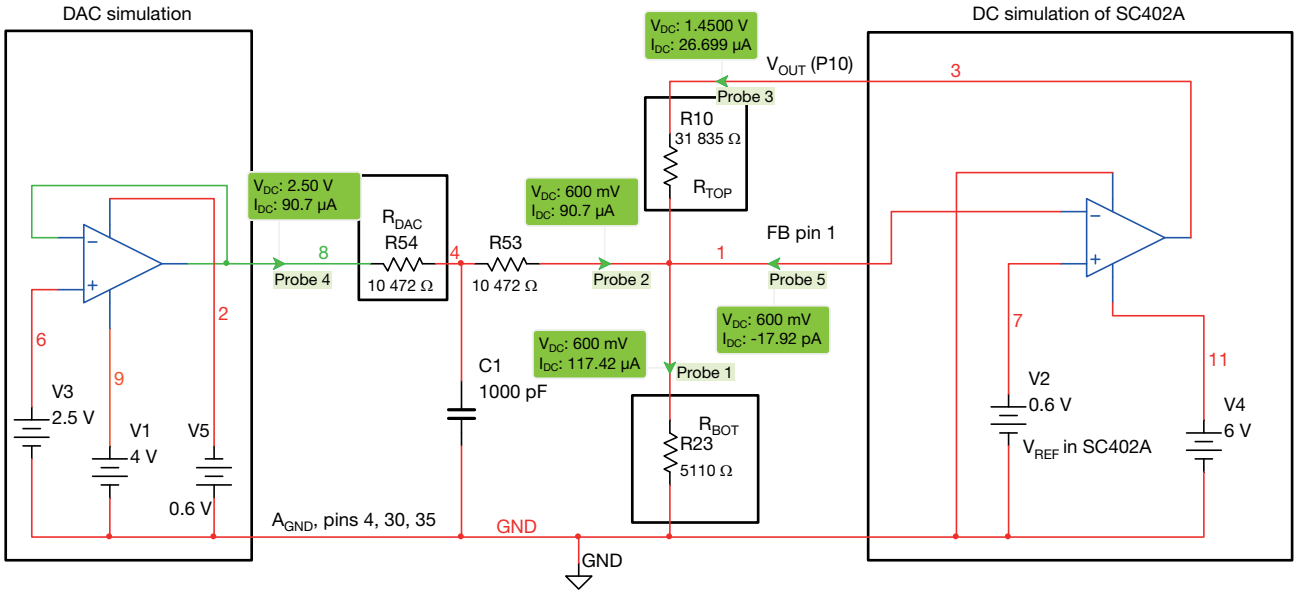

Fig. 33 - 1.5 V to 5.25 V Simulation

The calculator can be used to determine what the register settings are for the DAC. In this case, a 10-bit DAC allows a 3.7 mV per LSB adjustment of V_{OUT}.

Using the programmer's tool, the desired V_{OUT} values can be entered and the proper register values can be determined:

Convert regulator output voltage to DAC count	Regulator V_{OUT}	Count	Hex	
	2.5	741	$2E^5$	

Fig. 34 - Determining Register Settings for the DAC

Using the same circuit as above, a power rail for a bridge-based sensor can also be set up. In this case bits would be added to the DAC based on calibration needs.

Input DAC or voltage source parameters			
DAC bits (number)	DAC LSB (V)	1 DAC LSB adjust in SiC4XX V_{OUT} (V)	Total count (theoretical number of voltage steps from DAC) (number)
14	0.000153	0.000231934	16384

Fig. 35 - More DAC Bits Yields Increased Resolution in V_{OUT} Adjustability

In this circuit regulation is 1.480 V at 0 A and 1.459 V at 6 A; 5.309 V at 0 A and 5.288 V at 6 A.

AVS / DVS and Margining Circuits for Vishay Power ICs SiC40X Series SMPS Regulators

How to Obtain Exacting Resistor Values

In each of these designs it is critical that the resistor values for R_{TOP}, R_{BOT}, and R_{DAC} be quite precise. The ohmic value requirements of these resistors can vary greatly over the design possibilities. 0.1 % resistors may not meet the designer's requirements.

In these instances, there is a useful tool by which a parallel or series combination of 1 % resistors can be determined that will meet the design goal.

It is located at jansson.us/resistors.html.

Here is an example of the calculation of R_{TOP}, R10, from circuit 3 in Fig. 33, using the URL above:

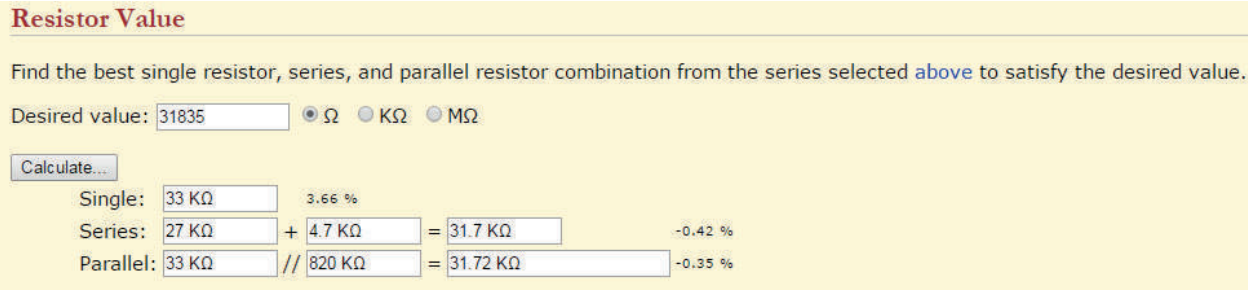

Fig. 36 - Precision Resistor Calculator

In this case R_{TOP} would consist of a 33 kΩ, 1 % resistor in parallel with an 820 kΩ, 1 % resistor. If both resistors were exactly at their stated values, the final parallel value would be off by -0.35 %.

There are also highly precise 0.01 % resistors with very low temperature coefficients that come in non-standard values and are made to order, such as the PLT series from Vishay (see www.vishay.com/doc?60030).

THE PROTOTYPE

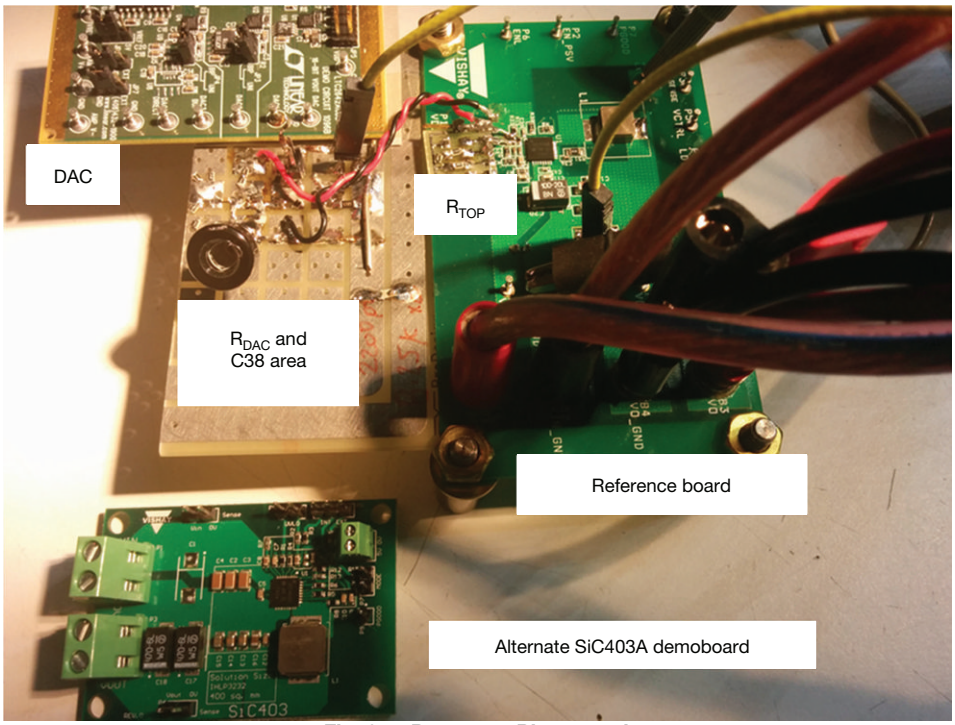

Fig. 37 - Prototype Photograph