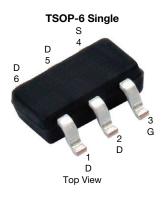


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Vishay Siliconix

Automotive P-Channel 40 V (D-S) 175 °C MOSFET



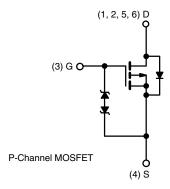
Marking Code: 8W

PRODUCT SUMMARY					
V _{DS} (V)	-40				
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.061				
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.093				
I _D (A)	-6.9				
Configuration	Single				

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified c
- 100 % R_q and UIS tested
- Typical ESD protection 800 V
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>





ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free and halogen-free	SQ3419AEEV (for detailed order number please see www.vishay.com/doc?79771)

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	-40	V	
Gate-source voltage		V _{GS}	± 12	V	
Continuous drain current	T _C = 25 °C		-6.9		
	T _C = 125 °C	I _D	-4	А	
Continuous source current (diode conducti	on)	I _S	-6.3		
Pulsed drain current		I _{DM}	-27		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	-18		
Single pulse avalanche energy	L = U. I MIH	E _{AS}	16.7	mJ	
Manifestura disabilità a	T _C = 25 °C	В	5	W	
Maximum power dissipation ^a	T _C = 125 °C	P_{D}	1.6		
Operating junction and storage temperature	e range	T _J , T _{sta}	-55 to +175	°C	

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	LIMIT	UNIT				
Junction to ambient	PCB mount b	R_{thJA}	110	°C/W			
Junction to case (drain)		R _{thJF}	30	G/VV			

Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. When mounted on 1" square PCB (FR4 material).
- c. Parametric verification ongoing.



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$		-40	-	-	.,,
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = -250 μA	-1.5	-2.0	-2.5	V
Coto Corres Lockson		V _{DS} =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$		-	± 2	μA
Gate-Source Leakage	l _{GSS}		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 30	mA
			$V_{DS} = -40 \text{ V}$	-	-	-1	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	$V_{DS} = -40 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$	ı	-	-50	μA
_		V _{GS} = 0 V	$V_{DS} = -40 \text{ V}, T_{J} = 175 ^{\circ}\text{C}$	-	-	-150	
On-State Drain Current a	I _{D(on)}	V _{GS} = -10 V	$V_{DS} = -5 V$	-10	-	-	Α
		V _{GS} = -10 V	I _D = -2.5 A	-	0.048	0.061	
Drain-Source On-State Resistance a	R _{DS(on)}	V _{GS} = -10 V		-	0.070	-	Ω
	(-::,		I _D = -2.5 A, T _J = 175 °C	-	0.081	- 0.000	
Farmend Transport division as b		$V_{GS} = -4.5 \text{ V}$ $I_D = -2 \text{ A}$		-	0.077	0.093	
Forward Transconductance ^b Dynamic ^b	9fs	V _{DS} =	= -15 V, I _D = -4 A	-	10	-	S
•		1			l		1
Input Capacitance	C _{iss}	_		-	733	975	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = -20 \text{ V, f} = 1 \text{ MHz}$	-	130	175	pF
Reverse Transfer Capacitance	C _{rss}			ı	84	115	
Total Gate Charge ^c	Qg			-	8.4	12.5	
Gate-Source Charge ^c	Q_{gs}	$V_{GS} = -4.5 \text{ V}$	$V_{DS} = -20 \text{ V}, I_{D} = -4 \text{ A}$	-	2.4	-	nC
Gate-Drain Charge ^c	Q_{gd}			-	4.1	-	
Gate Resistance	Rg	f = 1 MHz		2.6	5.3	7.9	Ω
Turn-On Delay Time ^c	t _{d(on)}			-	9	12	
Rise Time ^c	t _r	V_{DD} = -20 V, R_L = 5 Ω I_D \cong -4 A, V_{GEN} = -10 V, R_g = 1 Ω		-	24	32	- ns
Turn-Off Delay Time c	t _{d(off)}			-	26	34	
Fall Time c	t _f			-	31	41	
	actoristics b	1			ı		
Source-Drain Diode Ratings and Chara	acteriotics						
Source-Drain Diode Ratings and Chara Pulsed Current ^a	I _{SM}			-	-	-27	Α

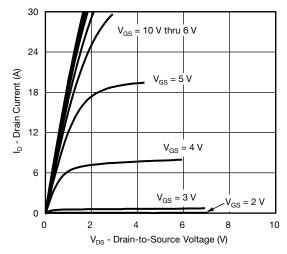
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

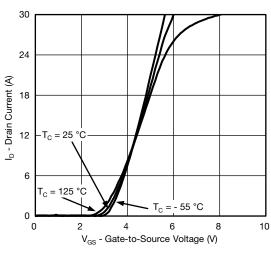
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



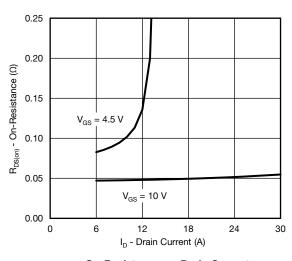
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



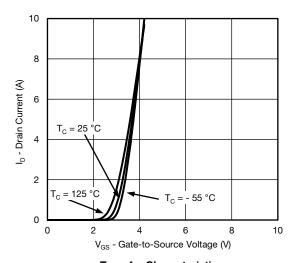
Output Characteristics



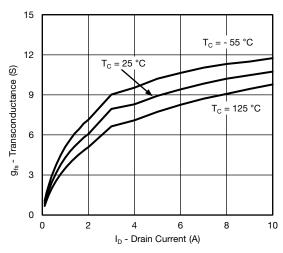
Transfer Characteristics



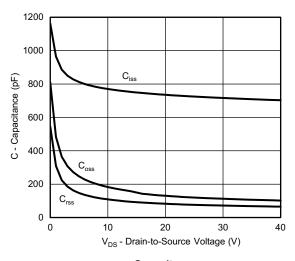
On-Resistance vs. Drain Current



Transfer Characteristics



Transconductance

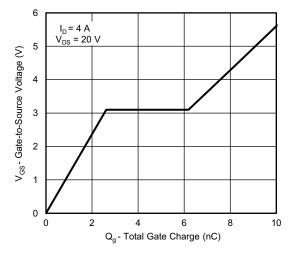


Capacitance

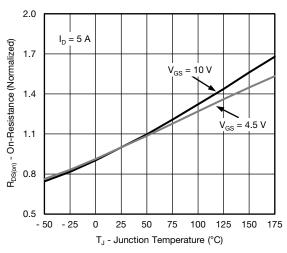
For technical questions, contact: automostechsu



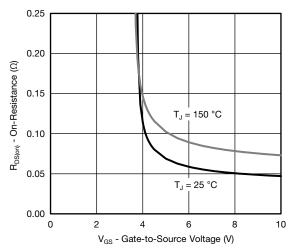
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



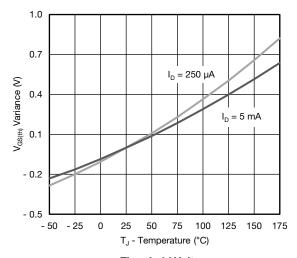
Gate Charge



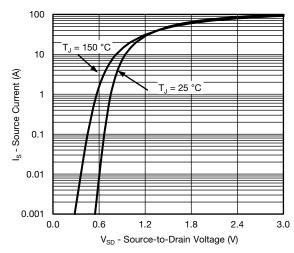
On-Resistance vs. Junction Temperature



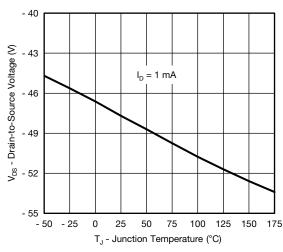
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



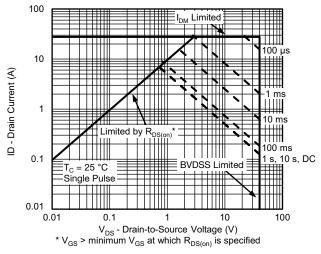
Source Drain Diode Forward Voltage



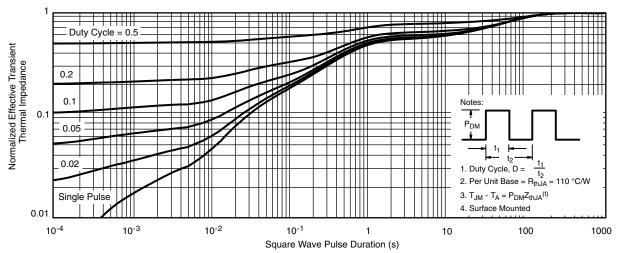
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



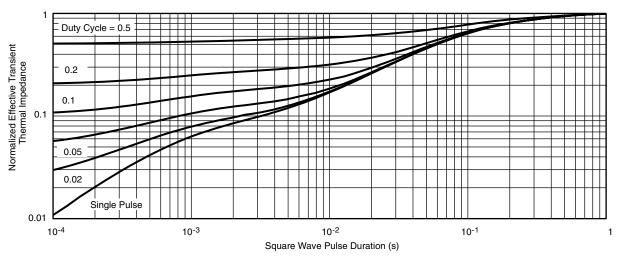
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg265332.





TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C





5-LEAD TSOP







	MIL	LIMETER	RS	INCHES				
Dim	Min	Nom	Max	Min	Nom	Max		
Α	0.91	-	1.10	0.036	-	0.043		
A ₁	0.01	-	0.10	0.0004	-	0.004		
A ₂	0.90	-	1.00	0.035	0.038	0.039		
b	0.30	0.32	0.45	0.012	0.013	0.018		
С	0.10	0.15	0.20	0.004	0.008			
D	2.95	3.05	3.10	0.116 0.120		0.122		
E	2.70	2.85	2.98	0.106	0.112	0.117		
E ₁	1.55	1.65	1.70	0.061	0.065	0.067		
е		0.95 BSC			0.0374 BSC			
e ₁	1.80	1.90	2.00	0.071	0.075	0.079		
L	0.32	-	0.50	0.012	-	0.020		
L ₁	0.60 Ref			0.024 Ref				
L ₂	0.25 BSC			0.010 BSC				
R	0.10	-	-	0.004	-	-		
θ	0°	4°	8°	0°	4°	8°		
θ1	7° Nom			7° Nom				
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540								

Document Number: 71200 18-Dec-06



Recommended Land Pattern For TSOP-5L / TSOP-6L



Note

• All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010



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