Dual N-Channel 20 V (D-S) MOSFET

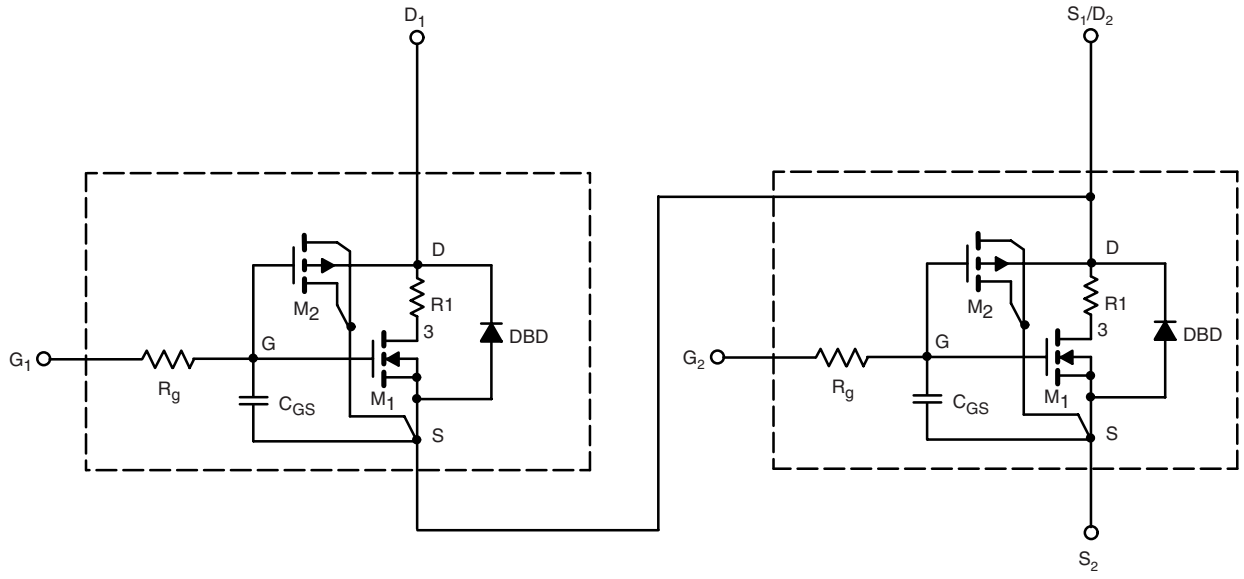
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

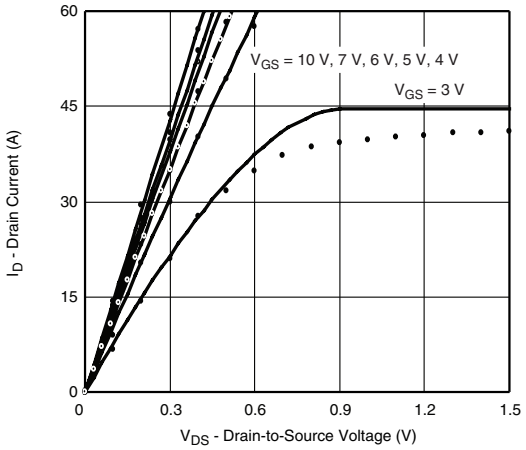
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	Ch-1	1.3	-	V
			Ch-2	1.6	-	
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A	Ch-1	0.007	0.007	Ω
		V_{GS} = 10 V, I_D = 20 A	Ch-2	0.0044	0.0047	
		V_{GS} = 4.5 V, I_D = 10 A	Ch-1	0.0089	0.0088	
		V_{GS} = 4.5 V, I_D = 15 A	Ch-2	0.0055	0.0054	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 15 A	Ch-1	48	60	S
		V_{DS} = 10 V, I_D = 20 A	Ch-2	72	100	
Diode Forward Voltage[a]	V_{SD}	I_S = 2 A, V_{GS} = 0 V	Ch-1	0.74	0.80	V
		I_S = 2.3 A, V_{GS} = 0 V	Ch-2	0.72	0.80	
Dynamic[a]						
Input Capacitance	C_{iss}	Channel 1 V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz Channel 2 V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	1290	1300	pF
			Ch-2	3860	3860	
Output Capacitance	C_{oss}		Ch-1	293	290	
			Ch-2	765	760	
Reverse Transfer Capacitance	C_{rss}		Ch-1	133	132	
			Ch-2	356	350	
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 15 A	Ch-1	20	20	nC
		V_{DS} = 10 V, V_{GS} = 10 V, I_D = 20 A	Ch-2	58	55	
		Channel 1 V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 15 A Channel 2 V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 20 A	Ch-1	9.9	9.5	
			Ch-2	28	27	
Gate-Source Charge	Q_{gs}		Ch-1	3.2	3.2	
			Ch-2	9.2	9.2	
Gate-Drain Charge	Q_{gd}		Ch-1	2.4	2.4	
			Ch-2	7.1	7.1	

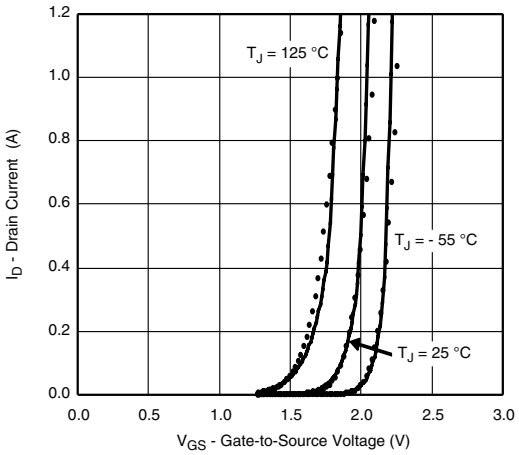
Notes

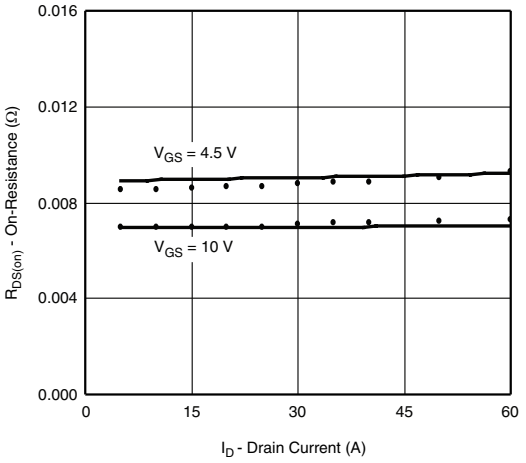
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

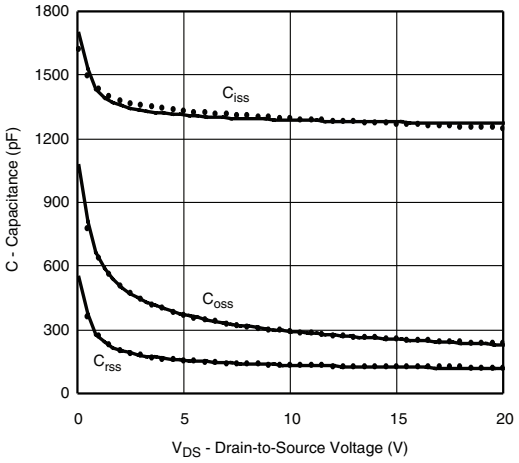
b. Guaranteed by design, not subject to production testing.

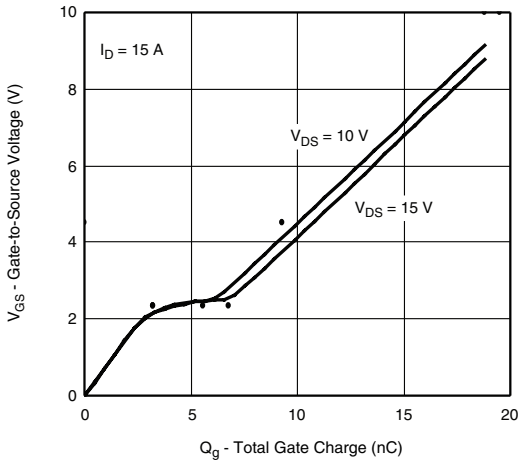
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted
Channel 1

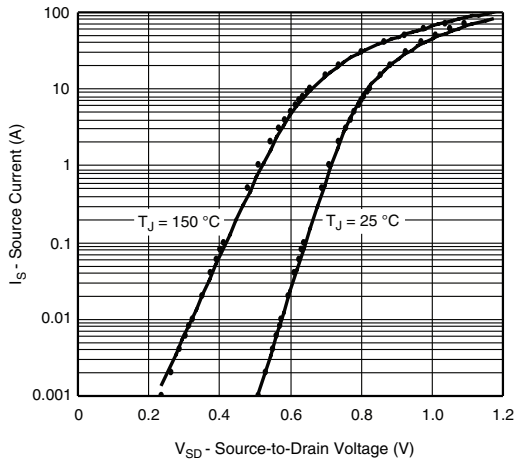








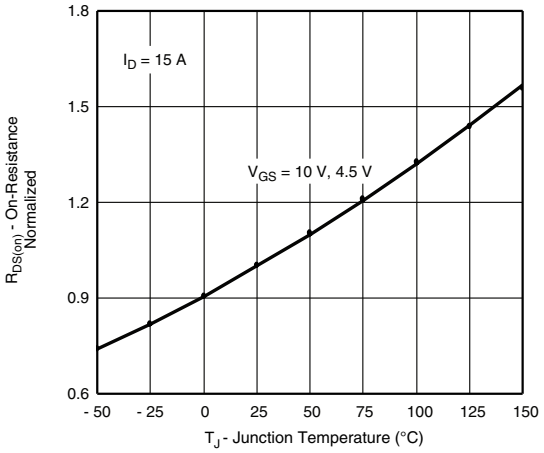


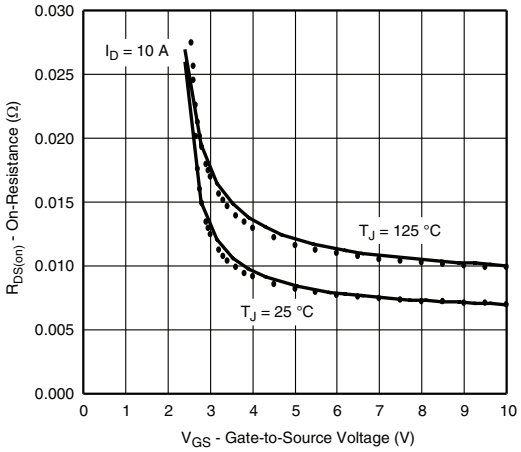


Note
Dots and squares represent measured data.

COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

Channel 1





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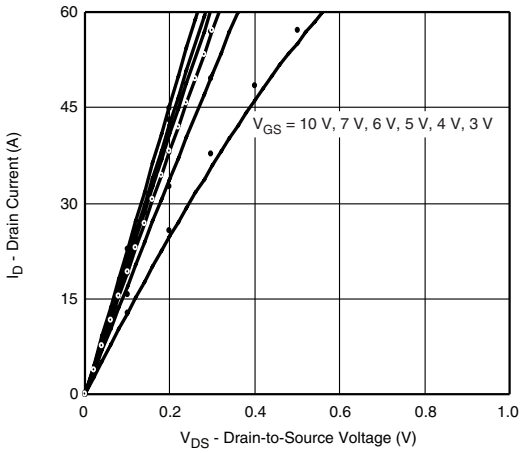
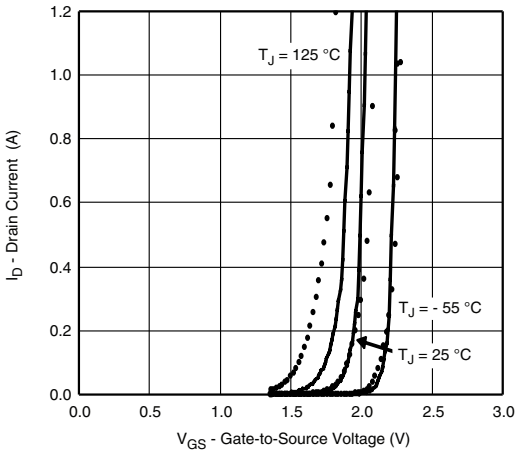
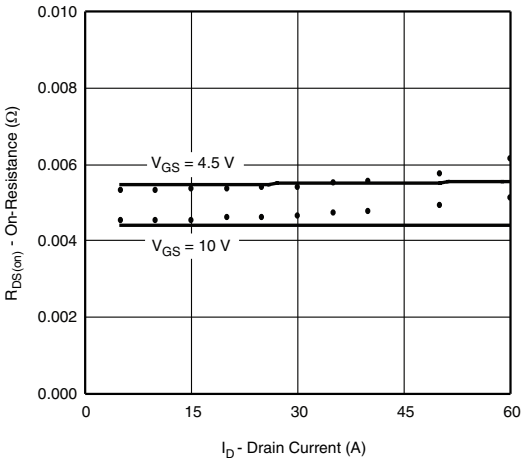
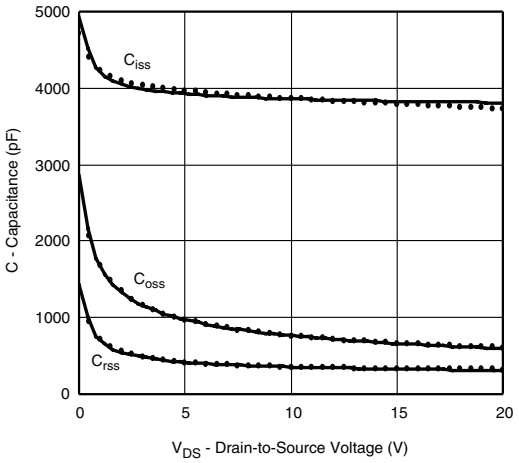
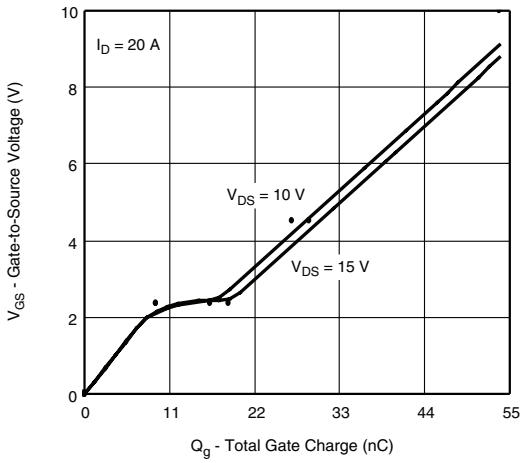
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted
Channel 2

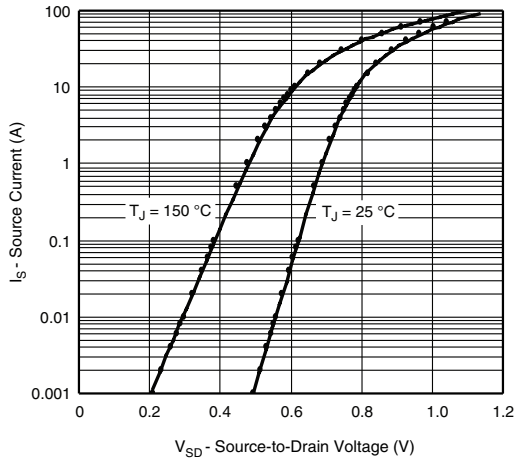












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