



How to Select the Right MOSFET for Power Factor Correction Applications

Power factor is the ratio of the real power (P = Watts) to the apparent power (VA = Volt Ampere); the goal is to achieve a power factor as close to 1 as possible. A load with a lower power factor draws more reactive current than a load with a higher power factor for the exact same output power. The higher current increases the energy lost within the system, and for utility companies, results in excessive wasted power in transmission. For this reason, a power factor correction (PFC) circuit block, shown in figure 1, is an important, and often mandatory, sub-system of any power supply with an output power of 75 W or more (per EN61000-3-2). A PFC circuit block is used to align the input line current with the AC voltage waveforms, and in most cases boosts the output voltage to a common 400 VDC. Figures 2 and 3 shows the impact of a PFC circuit on the line current and its harmonics.

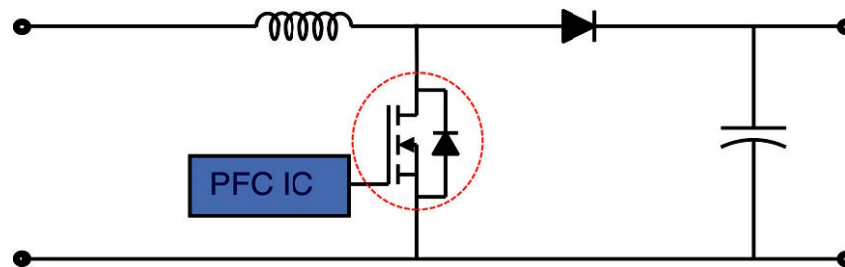


Fig. 1 - PFC Schematic

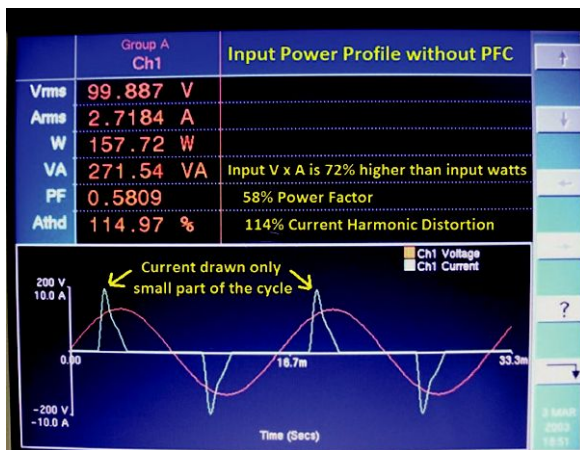


Fig. 2 - Line Voltage and Current without PFC

In figure 2, current is drawn from the AC supply only for a short duration of the cycle. This results in a poor power factor and excessive harmonics of 115 %. While the system draws only 158 W of usable power, 272 Volt-Amperes are circulated in the transmission system to deliver it.

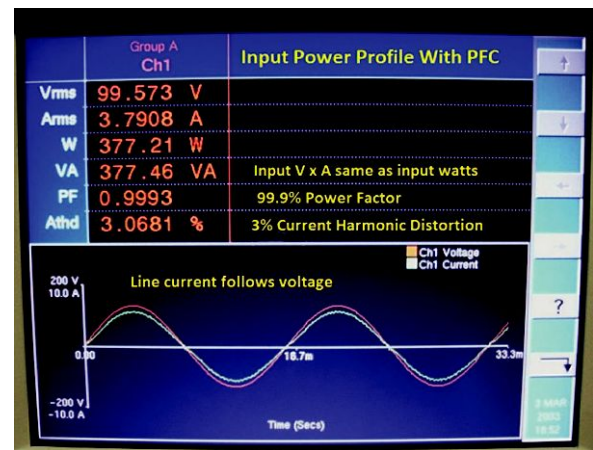


Fig. 3 - Waveforms with PFC

Figure 3 shows the benefits of implementing PFC using the same input power profile. With a power factor of 99.9 %, harmonics are down to 3 %. Current is drawn from the AC line throughout the cycle and no excessive Volt-Amperes are wasted.



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It should be noted that PFC and harmonic current reduction are not synonymous. For example, in a highly inductive load, the current may be a perfect sinusoid lagging the voltage. It will then have a poor power factor and high reactive power without any harmonics at all. Whereas a distorted waveform, rich in harmonic currents, usually has all the undesirable features. The PFC circuit corrects more than just the power factor; it reduces the harmonics. Today, there are different standards specifying the quality of power drawn by electronic equipment. EN61000-3-2 requires harmonic current reduction on all systems with input power of > 75 W. 80 Plus power supply certification requires a power factor of 0.9 or more.

In a PFC circuit, the MOSFET is responsible for approximately 20 % of all losses. By choosing the correct device, PFC efficiency can be greatly increased. One way to select the right MOSFET for a PFC circuit is by using an application-specific Figure of Merit (FOM) that is focused on minimizing total losses in the device. While it includes on-resistance ($R_{DS(on)}$) for conduction losses and gate charge (Q_g) for switching losses, the FOM is not a simple product of the two. In order to account for switching losses, a portion of the device's Q_{gs} and Q_{gd} , along with its output capacitance (C_{oss}), are used.

The four stages of a standard AC/DC power supply are:

- Input
- PFC Front End
- Converter
- Secondary

To meet 80 Plus Gold efficiency standards, the combined loss for all stages is ~ 12 % of the rated output power. The PFC MOSFET alone should be limited to around 2 % of the total output power or the package power limit, whichever is lower. The maximum power loss limits of “TO” packages are:

- TO-220 / TO-220F: 10 W/8 W
- TO-247: 20 W
- Super TO-247 / T_{max} : 25 W

So, the maximum package power limits that consist of both conduction and switching losses should not exceed the above levels. Conduction loss is a simple $I^2 \cdot R$ calculation that takes into account the $R_{DS(on)}$ of the device as well as its temperature coefficient. The switching losses need to take into account not only Q_g , Q_{gd} , and Q_{gs} , but also Q_{oss} , which is an integral function of C_{oss} .

The traditional FOM, $R_{DS(on)} (typ.) \cdot Q_g (typ.)$, does not take into account the C_{oss}/Q_{oss} of the device, which is a very important loss, especially at light loads where switching losses trump conduction losses. This component of the

switching loss is incurred both ways, as C_{oss} is charged when the device turns off and discharged when it is turned on, and has to be taken into account in the design. The larger the C_{oss}/Q_{oss} , the larger the switching losses. In addition, the Q_{oss} loss is fixed and independent of load, as can be seen by the standard equation $P_{oss} = \frac{1}{2} CV^2 \times F_{sw}$, where F_{sw} is the switching frequency.

In universal input power supplies, the PFC MOSFET is always subjected to the bulk DC bus voltage of 380 VDC to 400 VDC. As a result, the output switching loss can be a significant portion of the total losses. The C_{oss} of a high-voltage MOSFET (HVM) varies considerably with the applied V_{DS} . This variation is much wider for high-voltage Super Junction power MOSFETs than for planar types. To account for the non-linearity of the output capacitor, $P_{oss} = \frac{1}{2} C_{oer} \times V^2 \times F_{sw}$ may be used as the loss equation. C_{oer} is the effective capacitance that has the same stored energy and same losses as the integrated C_{oss} of the MOSFET, and is provided in the datasheets. So, the new FOM will now look like $R_{DS(on)} (typ.) \cdot (Q_{switch} (typ.) + Q_{oss})$, where Q_{switch} is a combination of Q_{gd} and Q_{gs} .

As an example, we will use a TO-220 device with a maximum package power loss of 10 W, and contribute 5 W to conduction losses and 5 W to switching losses. The C_{oss}/Q_{oss} losses would contribute to approximately 20 % of the overall package loss, or 40 % of the total switching losses, which is a large loss that is not taken into account with the standard FOM equation. With this in mind we have developed a list of components that we feel will achieve the highest efficiency for a PFC design based on the following operating conditions (see table 1) to help our customers develop the most efficient design possible.

TABLE 1 - POWER FACTOR CORRECTION DESIGN CONDITIONS

Input Voltage	100 V
Output DC Voltage	400 V
PFC Switching Frequency	65 kHz
MOSFET Drive Voltage	12 V
On/Off Gate Current Range	0.5 A (25 W) to 1.2 A (475 W)

The list of recommended devices includes an “x” in the “package” location. For the same set of electrical characteristics, a number of package options may be available per device. The packages used will depend on the power level as well as what MOSFET real estate is allowed. Figures 2 and 3 define the packages, current rating, voltage, and device technology of the different part numbers.

APPLICATION NOTE

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Definition: Vishay High-Voltage MOSFET Part Number: SiHxDDNFFG

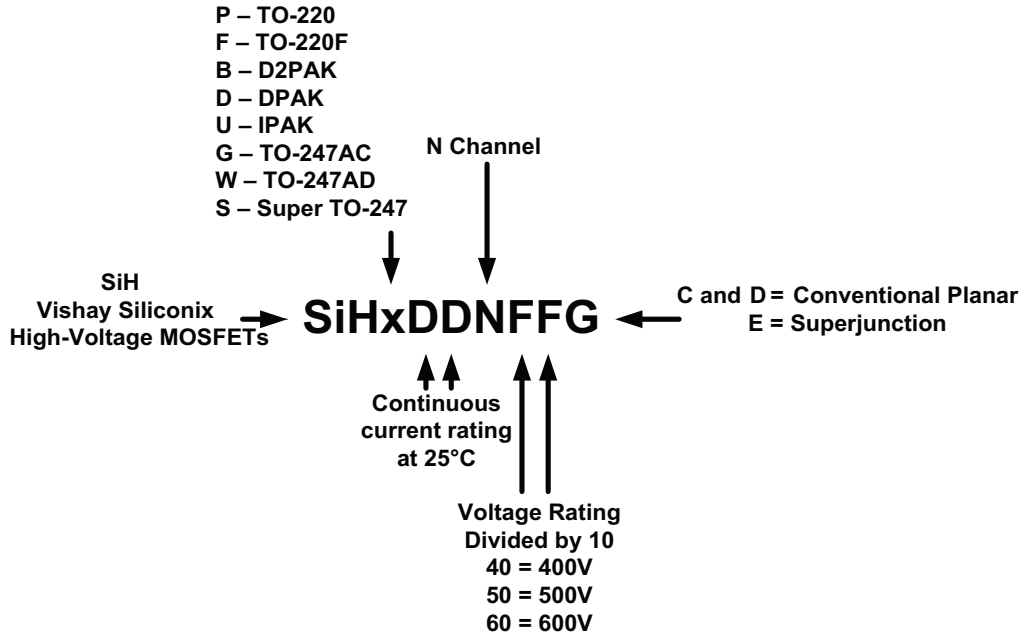


Fig. 4 - Part Numbers Definition

With many package options available, table 2 lists the recommended maximum power rating for the different package offerings.

TABLE 2 - RECOMMENDED POWER LEVELS BASED ON PACKAGE TYPE	
PACKAGES	RECOMMENDED MAXIMUM RATINGS ⁽¹⁾
DPAK (TO-252)	up to 25 W
IPAK (TO-251)	up to 75 W
D2PAK (TO-263)	up to 200 W
TO-220	up to 350 W ⁽²⁾
TO-220F	up to 350 W ⁽²⁾
TO-247AC	up to 1000 W
TO-247AD	up to 1000 W
Super TO-247	up to 1500 W

Note

- (1) If multi layer PCBs are used where heat sinking is enhanced then the package(s) can be used at higher power levels
- (2) If an interleaved PFC design is used then the output power can be up to 750 W (using two TO-220s). Paralleling two TO-220s or TO-220Fs will allow up to 750 W with a non-interleaved design.

With the design conditions, device part number understanding, and maximum recommended per package type, table 3 shows the respective devices for the different power levels.

This list shows many different devices. Depending on whether voltage, efficiency, or price is the higher concern you can pick and choose the device that best fits your application.

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TABLE 3 - POWER FACTOR CORRECTION MOSFET SELECTOR GUIDE

P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}	P _{out}
5 W	10 W	20 W	25 W to 50 W	75 W to 100 W	125 W	150 W	200 W to 250 W	300 W to 500 W	600 W	750 W to 1 kW	> 1 kW				
500 V	500 V	500 V	500 V	500 V	500 V	500 V	500 V	500 V	500 V	500 V	500 V	500 V	500 V	500 V	500 V
SiHx3N50D	SiHx5N50D	SiHx12N50C	SiHx12N50C	SiHx16N50C	SiHx14N50D	SiHx16N50C	SiHx18N50D	SiHx36N50D	SiHx33N60E	SiHx33N60E	SiHx33N60E	SiHx33N60E	SiHx33N60E	SiHx33N60E	SiHx33N60E
SiHx5N50D	SiHx8N50D	SiHx8N50D	SiHx8N50D	SiHx12N50C	SiHx14N50D	SiHx14N50D	SiHx16N50C	-	-	-	-	-	-	-	-
600 V	600 V	600 V	600 V	600 V	600 V	600 V	600 V	600 V	600 V	600 V	600 V	600 V	600 V	600 V	600 V
SiHx7N60E	SiHx7N60E	SiHx7N60E	SiHx7N60E	SiHx12N60E	SiHx12N60E	SiHx22N60E	SiHx22N60E	SiHx30N60E	SiHx33N60E	SiHx33N60E	SiHx33N60E	SiHx33N60E	SiHx33N60E	SiHx33N60E	SiHx33N60E
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
650 V	650 V	650 V	650 V	650 V	650 V	650 V	650 V	650 V	650 V	650 V	650 V	650 V	650 V	650 V	650 V
SiHx6N65E	SiHx6N65E	SiHx6N65E	SiHx6N65E	SiHx15N65E	SiHx15N65E	SiHx22N65E	SiHx22N65E	SiHx24N65E	SiHx47N65E	SiHx47N65E	SiHx47N65E	SiHx47N65E	SiHx47N65E	SiHx47N65E	SiHx47N65E
-	-	-	-	-	-	-	-	SiHx28N65E	-	-	-	-	-	-	-

Note: Devices with "x" can use multiple packages; ones with "C" and "S" must use the TO-247 and Super TO-247 type packages respectively.