# SPICE Device Model SiA906EDJ



Vishay Siliconix

# Dual N-Channel 20 V (D-S) MOSFET

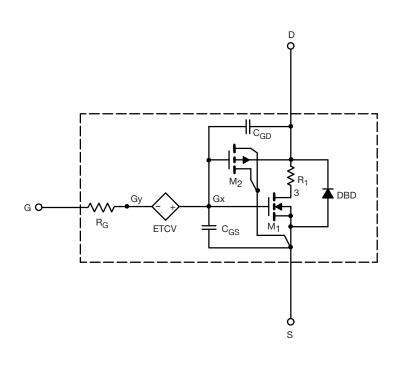
### DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC

### **CHARACTERISTICS**

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge



#### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	1	-	V
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 3.9 \text{ A}$	0.037	0.037	Ω
		$V_{GS} = 2.5 \text{ V}, \text{ I}_{D} = 3.3 \text{ A}$	0.050	0.051	
Forward Transconductance <sup>a</sup>	<b>g</b> fs	$V_{DS} = 10 \text{ V}, I_D = 3.9 \text{ A}$	12	14	S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 4.1 A	0.85	0.80	V
Dynamic <sup>b</sup>					
Input Capacitance	C <sub>iss</sub>	$V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz	348	350	pF
Output Capacitance	C <sub>oss</sub>		57	63	
Reverse Transfer Capacitance	C <sub>rss</sub>		33	37	
Total Gate Charge	Qg	$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 5.1 \text{ A}$	6.8	7.5	nC
Total Gate Charge		$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 5.1 \text{ A}$	3.3	3.5	
Gate-Source Charge	Q <sub>gs</sub>		0.95	0.95	
Gate-Drain Charge	Q <sub>gd</sub>		0.75	0.75	

Notes

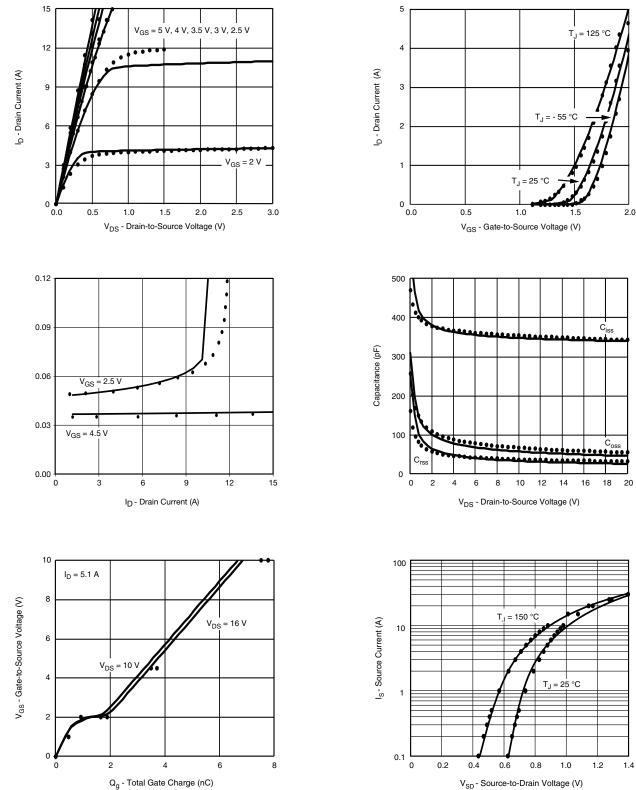
a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

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## COMPARISON OF MODEL WITH MEASURED DATA (T<sub>J</sub> = 25 °C, unless otherwise noted)



#### Note

• Dots and squares represent measured data.

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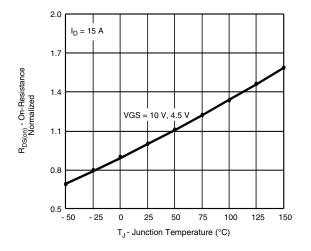
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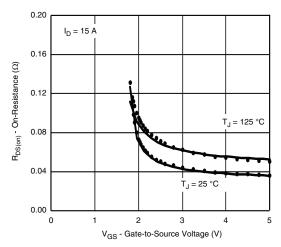
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### COMPARISON OF MODEL WITH MEASURED DATA (T<sub>J</sub> = 25 °C, unless otherwise noted)





Note

Dots and squares represent measured data.

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